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A Test Environment for the ATLAS Calorimeter Trigger

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A Test Environment for the ATLAS Calorimeter Trigger

This thesis describes the development of a test environment for the ATLAS Level-1 Calorimeter Trigger Pre-Processor. The Pre-Processor system performs complex digital data processing of analog calorimeter trigger tower signals. In order to increase the flexibility of the test system, a modular approach was chosen.

A commercial graphics card is programmed to accurately emulate calorimeter test beam pulses. These signals form the input to a fully assembled Multi-Chip Module (MCM) which incorporates the main functionality of the Pre-Processor system. A testboard that carries the MCM provides the necessary interfaces to the remaining test setup. Three printed circuit boards constitute the data sink for the MCM output. A FPGA on each board performs the data transfer from the receiver card to the VMEbus from which all test data can be read out.

The data obtained during a first series of tests are analyzed and found to be in good agreement with the expected response of the MCM to an analog stimulus.

Eine Testumgebung für den ATLAS Kalorimeter Trigger

Die vorliegende Arbeit beschreibt die Entwicklung einer Testumgebung für den ATLAS Level-1 Kalorimeter Trigger Prä-Prozessor, dessen Aufgabe die digitale Verarbeitung analoger Kalorimeterpulse ist. Um ein hohes Maß an Flexibilität zu gewährleisten, wurde ein modulares Testsystem entworfen.

Eine handelsübliche Grafikkarte wird eingesetzt, um auf der Basis von Testdaten realistische Kalorimeterpulse zu erzeugen. Diese bilden ihrerseits das Eingangssignal für die zu testende Hauptkomponente des Prä-Prozessor Systems: das Multi-Chip Modul (MCM). Ein Testboard dient als Träger für das MCM und stellt die notwendigen Schnittstellen zu dem übrigen Testsystem zur Verfügung. Drei Platinen, die mit je einem FPGA bestückt sind, empfangen die Ausgabe des MCM Testboards und ermöglichen das Auslesen der Daten über den VMEbus.

Die Auswertung erster Tests ergibt eine gute Übereinstimmung der Daten mit der erwarteten Antwort des MCMs auf einen analogen Stimulus.

Contents

Introduction

Although the concept of indivisible matter goes back into the time of ancient Greece, the scientific basement was only established in the 19th century. The first constituent of atoms, the electron, was discovered by J.J. Thomson in 1897. Another experimentally confirmed particle was the photon (1905), first postulated by M. Planck in 1900. In the following decades, more particles like the proton (1919) and the neutron (1932) were identified. To justify the observation of a continuous energy spectrum of electrons emitted in nuclear β decay, an "invisible" particle, the neutrino, was postulated by W. Pauli in 1930. Subsequently, numerous particles were discovered, *e.g.* the muon (1937), the pion (1947), the Λ (1951), and the η (1961), constantly enlarging the number of known particles. In 1964, M. Gell-Mann and G. Zweig proposed the existence of fractionally charged particles called quarks. They predicted the Ω particle that was discovered in the same year. Experiments which supported the quark idea were carried out in Stanford: deep inelastic ep scattering confirmed the existence of pointlike particles called partons by R. Feynman. Some years later, it appeared that these partons are indeed identical to quarks. However, these quarks had never been observed as free particles. A solution to this dilemma is the idea of quark confinement introduced in the theory of strong interactions, Quantum Chromodynamics (QCD), that was inspired by the theory of Quantum Electrodynamics (QED). The latter describes the electromagnetic interaction between charged particles.
As gluons do not couple to neither muons nor electrons nor neutrinos, QCD cannot explain the muon decay into an electron and two neutrino-type particles. Since the coupling of this decay is considerably smaller than that of strong or electromagnetic decays, this interaction is called "weak". In 1968, S. Glashow, S. Weinberg, and A. Salam succeeded in unifying the weak and the electromagnetic interaction into the electroweak theory.
During the 1970s, the combination of QCD and the electroweak theory evolved to become the Standard Model of particle physics. Besides the gluon as the mediator of the strong interaction and the photon as mediator between charged particles, three further mediators are introduced to describe weak interactions: the Z^0 and the $W^{\pm}$. The discovery of the Z^0 and the $W^{\pm}$ in 1983 is one the most convincing experimental evidence for the validity of the Standard Model. However, one particle predicted by the Standard Model has not been observed yet: the Higgs particle.
Encouraged by the immense success of the Standard Model during the last decades, particle physicists are working on new experiments to "hunt" the Higgs particle. One of these experiments, ATLAS, is currently being built to investigate proton-proton collisions within the Large Hadron Collider (LHC), a particle accelerator presently under construction. Apart from the search for the Higgs particle, the experiment will gain insight into

unprecedented energy ranges which could lead to the discovery of physics beyond the Standard Model.
The first chapter of this thesis presents an introduction to the Standard Model of particle physics and to possible physics beyond the Standard Model. An overview of the LHC is given in the next chapter with emphasis placed on the ATLAS experiment and its subdetector systems. Chapter 3 introduces the ATLAS Trigger system and focuses on the Level-1 Calorimeter Trigger in particular while the following chapter deals with the Level-1 Calorimeter Trigger Pre-Processor. The development of a test environment for the Pre-Processor is presented in Chapter 5 followed by a description the software and firmware developed for the test system in Chapter 6. The final chapter summarizes and interprets the measurements obtained during a first series of tests.

Chapter 1

Physical Context

1.1 The Standard Model of Particle Physics

1.1.1 Introduction to the Standard Model

The Standard Model of particle physics is a local gauge field theory that evolved during the last decades. It will only be briefly summarized in this section. More profound descriptions of the Standard Model can be found *e.g.* in [1] or [2]. Its strength certainly is to describe the properties of particles and the resulting interactions between them with unprecedented accuracy, although many parameters, like the masses of particles, have to be phenomenologically introduced into the theory. Up to present, no experiment has found evidence of phenomena which cannot be explained within the framework of the Standard Model.
According to the Standard Model, matter consists of twelve fundamental particles, namely six quarks, which are the constituents of all hadrons, and six leptons. Additionally, each of these twelve particles has its corresponding antiparticle. All particles can be classified as either one of the following types:

1. Fermions carry half-integer spins. All quarks and leptons belong to this group of particles.

2. Bosons, *e.g.* all mediator particles of the four fundamental forces (gravity, electromagnetic, weak, and strong force), have integer spins.

Furthermore, leptons can be classified into three families or flavors which differ mainly by the different masses of the involved particles. Table 1.1 summarizes the most important properties of the leptons. The corresponding values for the antiparticles can easily be obtained by adjusting quantum numbers accordingly, *i.e.* in this case by simply multiplying the electric charge by -1. Recent discoveries [3] indicate that neutrinos seem to flavor oscillate over time. The possibility of this phenomenon, while not yet completely understood theoretically, is the reason for the undetermined entries in the last column of Table 1.1.
The same categorization is done for quarks (see Table 1.2). To obtain the correct values for the corresponding antiquarks, some quantum numbers have to be adjusted, *i.e.* one

Generation	Flavor	El. Charge	Mass $[MeV/c^2]$	Mean Lifetime $[s]$
I	ν_e	0	$< 3 \times 10^{-6}$	?
	e^-	-1	0.511	∞
II	ν_μ	0	< 0.19	?
	μ^-	-1	105.7	2.197×10^{-6}
III	ν_τ	0	< 18.2	?
	τ^-	-1	1776.99	290.6×10^{-15}

Table 1.1: Fundamental properties of leptons [4].

Generation	Flavor	Charge	Mass $[MeV/c^2]$	Color
I	*up*	$\frac{2}{3}$	1..5	r, g, b
	down	$-\frac{1}{3}$	3..9	r, g, b
II	*charm*	$\frac{2}{3}$	$1.15..1.35 \times 10^3$	r, g, b
	strange	$-\frac{1}{3}$	75..170	r, g, b
III	*top*	$\frac{2}{3}$	$170..179 \times 10^3$	r, g, b
	bottom	$-\frac{1}{3}$	$4..4.4 \times 10^3$	r, g, b

Table 1.2: Fundamental properties of quarks [4].

has to invert the color charge of quarks (*e.g. red* becomes $\overline{red}$) and multiply the electric charge by -1.
All Interactions between particles are the result of the forces acting on them. All three forces incorporated in the Standard Model are mediated by spin-1 gauge bosons:

1. The strong force is mediated by the massless gluon which couples to the color charge (red, green or blue) carried by all quarks. Since gluons are color charged themselves (they carry a color and an anticolor), they can interact with each other resulting in a finite range of the strong force even though gluons are massless. The theory describing the strong interaction is called Quantum Chromodynamics (QCD) [2].

2. The massless photon is the mediator of the electromagnetic force which couples to the electric charge. The electromagnetic interaction is described by the theory of Quantum Electrodynamics (QED) first developed by R. Feynman in 1948 [2].

3. The weak interactions are mediated by the exchange of either a neutral vector boson Z^0 ($m_Z = 91.19\,GeV/c^2$, [4]) or one of the charged vector bosons W^+ or W^- ($m_{W^\pm} = 80.43\,GeV/c^2$, [4]). These massive bosons couple to the weak charge which is carried by all leptons and quarks.

In 1968, Glashow, Weinberg and Salam [1] were able to unify the electromagnetic and weak interactions using a single mathematical framework: the theory of electroweak interactions. The relative strengths of the fundamental forces and their respective ranges are shown in Table 1.3. Gravity, by far the weakest force, is not included in the Standard Model.

Interaction	Mediator	Acts on	Range $[m]$	Rel. Strength
Strong	*Gluon* (g)	*color charge*	10^{-15}	1
Electromagnetic	*Photon* (γ)	*el. charge*	∞	10^{-2}
Weak	Z^0, $W^{\pm}$	*weak charge*	10^{-18}	10^{-5}
Gravitational	*Graviton*[1] (G)	*mass*	∞	10^{-40}

Table 1.3: Relative strengths and ranges of the four fundamental forces [5].

1.1.2 The Higgs Mechanism

To explain the masses of the Z^0 and $W^{\pm}$ bosons, a spontaneous symmetry-breaking was postulated in the unification scheme of the electroweak theory. This formalism could also lead to the correct masses of all other particles, the alternative being to introduce a free parameter for each particle mass into the Standard Model. This mass creating model is called the Higgs mechanism [2]. A direct consequence of this mechanism is the introduction of a neutral spin-0 scalar particle, the Higgs boson H. All of its properties can be calculated in terms of its mass which is a free parameter in the Standard Model. As opposed to all mentioned quarks, leptons and mediators (except for the graviton), the Higgs particle has not been experimentally observed yet. Direct measurements exclude Higgs masses below $114\,GeV/c^2$ [6]. The most relevant decay channels for the Higgs boson are summarized in Figure 1.1 as a function of the Higgs boson mass [7]. For masses below $140\,GeV/c^2$, decays to fermion anti-fermion pairs dominate, with $H \to b\bar{b}$ having a branching ratio of about 0.85. For larger masses, the Higgs boson decays most probably into W^+W^- or Z^0Z^0.

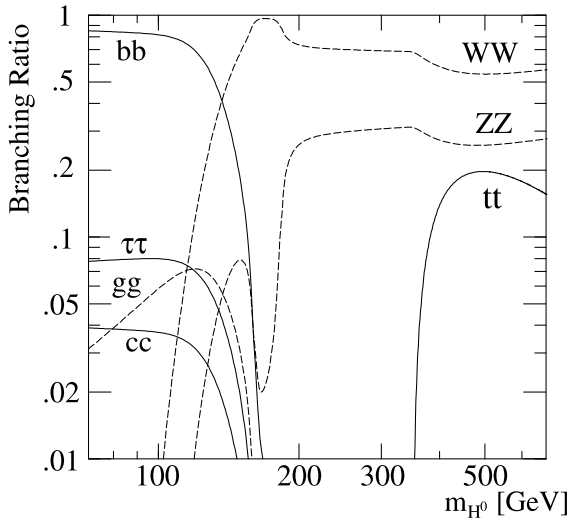

Figure 1.1: Branching ratios for the main decay modes of the Standard Model Higgs boson as a function of its mass [7].

[1] So far, there has not been any experimental evidence for the existence of the graviton.

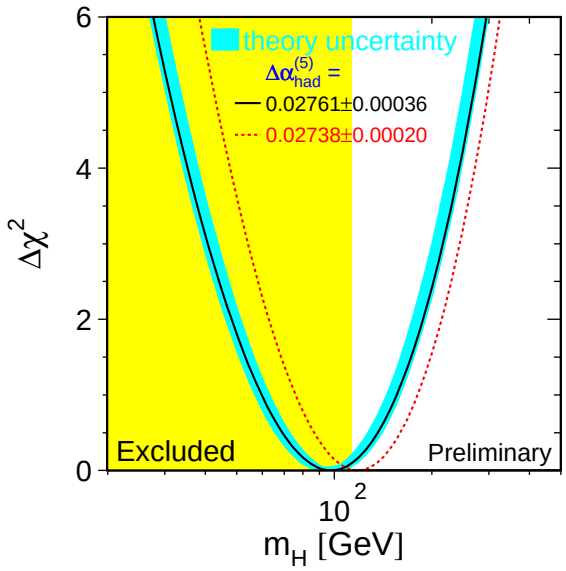

Figure 1.2: $\triangle\chi^2$ *vs.* m_H curve [8]. The solid line is the result of the fit using all available data; the band represents an estimate of the theoretical error due to missing radiation corrections. The shaded area shows the 95% CL exclusion limit from the direct search for the Higgs boson [6]. The dashed curve is the result obtained using another evaluation of $\Delta\alpha^{(5)}_{had}$ which is the contribution of the light quarks to the photon vacuum polarization.

Figure 1.2 summarizes the results of several experiments [6] performing precision measurements of electroweak parameters in combination with theoretical expectations: the most probable mass for the Higgs boson is about $100\,GeV/c^2$. The current upper limit is $m_H = 196\,GeV/c^2$ with a confidence level (CL) of 95%.

1.1.3 Proton-Proton Physics

Protons consist of partons which are identified as three valence quarks (up, up, down), a sea of virtual quarks, and gluons. As mentioned previously, those partons interact via the strong force and therefore QCD is the appropriate theory to describe the behavior of partons inside the proton itself as well as for interactions between partons of different protons. Unfortunately, QCD predictions can only be calculated perturbatively in the short-distance region since the coupling grows much stronger at greater distances.

Proton-Proton Scattering

In most cases, two protons will scatter off each other elastically, which means that the internal structure of both protons remains stable throughout the interaction. Corresponding

to a low momentum transfer, the signature of such events are marginally deflected protons, *i.e.* the scattered proton lies in proximity of the original beam axis. Deep inelastic scattering, *i.e.* two partons colliding or even annihilating each other, will only take place in a tiny fraction of all collisions. Characteristic signatures of such deep inelastic scattering events are particle jets[2] in or near the plane perpendicular (transverse) to the beam axis, corresponding to a high momentum transfer between two partons. The center of mass energy available for the production of new particles, for example Higgs bosons, is not equal to the total center of mass energy $\sqrt{s}$ of the overall process since the involved partons carry just a fraction x_1 and x_2 of the total momentum of their respective proton. These fractions can be calculated with the experimentally measured structure function $F_2(x_i, Q^2)$, with $i = 1, 2$ and Q being the momentum transfer between the two partons. Therefore, the amount of energy left for daughter particles is reduced to $\sqrt{x_1 x_2 s} \approx 0.1\sqrt{s}$ [5].

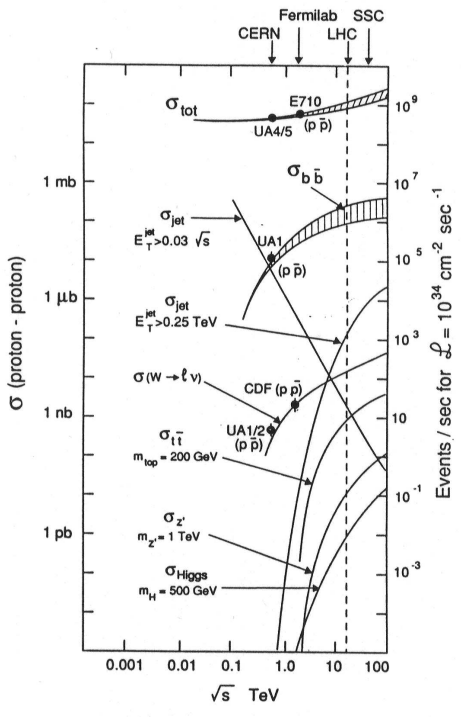

Figure 1.3: Cross-section for different proton-proton scattering events as a function of center of mass energy [9].

Figure 1.3 shows the partial cross-sections for heavy quark and Higgs boson production as well as the total cross-section for proton-proton scattering as a function of the total center of mass energy $\sqrt{s}$. Some physically interesting processes, like the direct production of the Higgs boson, only contribute an extremely small part to the overall cross-section. The fraction of the cross-sections in this case is: $\sigma_{Higgs}/\sigma_{Total} \approx 10^{-11}$ [9].

[2] A jet is the conglomeration of several hadrons that are produced during the hadronization process of a single quark.

1.2 Physics beyond the Standard Model

Despite the fact that the Standard Model has provided physicists with a powerful tool to describe and understand experimental particle physics data throughout the last decades, important issues in the Standard Model remain unexplained. Many parameters have to be introduced into the theory, *e.g.* no explanations for the strengths of the different coupling constants or for the existence of exactly three families of quarks and leptons are given. A theoretical approach of extending the Standard Model is the concept of Supersymmetry (SUSY) which introduces a symmetry between fermions and bosons: all fermions are given bosonic partners differing by spin-$\frac{1}{2}$ and bosons are given fermionic partners also differing by spin-$\frac{1}{2}$ from their supersymmetric partner. Examples would be a spin-0 "squark" as bosonic partner for a quark or "gluinos" as spin-$\frac{1}{2}$ supersymmetric partners of gluons. As a consequence, the Higgs sector would change considerably: instead of one Higgs particle, four Higgs particles are expected in this model [10]. However, no supersymmetric particle has been detected so far. This leads to the conclusion that the assumed fermion-boson symmetry has to be broken in order to explain the obvious mass differences between the known particles and their partners. If the SUSY approach turns out to be correct, theorists could make a step towards the unification of the strong and the electroweak theory, possibly leading to a Grand Unified Theory (GUT) which might also include gravity in the future.

Chapter 2

The ATLAS Experiment at the Large Hadron Collider

In 2007, the Large Hadron Collider (LHC) will commence operation at the research facility of the European Organization for Nuclear Research (CERN[1]) close to Geneva, Switzerland. Currently under construction, the LHC will meet the stringent requirements dictated by the goal of reaching unprecedented insight into high energy, *i.e.* small scale, physics and possibly discover new physics (as mentioned in Section 1.2). This chapter describes the design of the LHC as well as the ATLAS experiment which is one out of four experiments to be carried out at CERN.

2.1 The Large Hadron Collider

It was decided to use the existing Large Electron Positron Collider (LEP) tunnel with a circumference of about 27 km to host the LHC. Figure 2.1 shows the infrastructure needed to inject pre-accelerated protons into the LHC accelerator ring, starting with the 50 MeV Linac (Linear accelerator) followed by the 1.4 GeV Proton Synchrotron (PS) booster, the 25 GeV PS, and finally the 450 GeV Super Proton Synchrotron (SPS) [11].

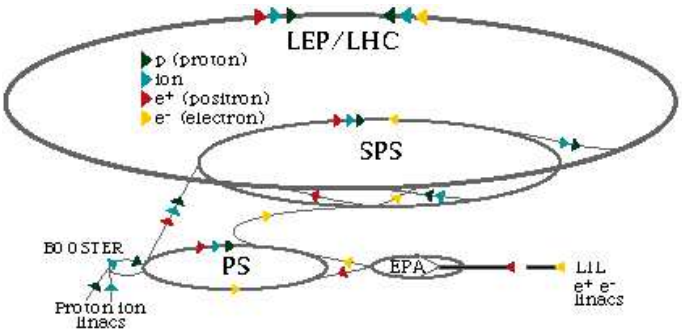

Figure 2.1: The accelerator chain at CERN [11].

[1]Conseil Européen pour la Recherche Nucléaire.

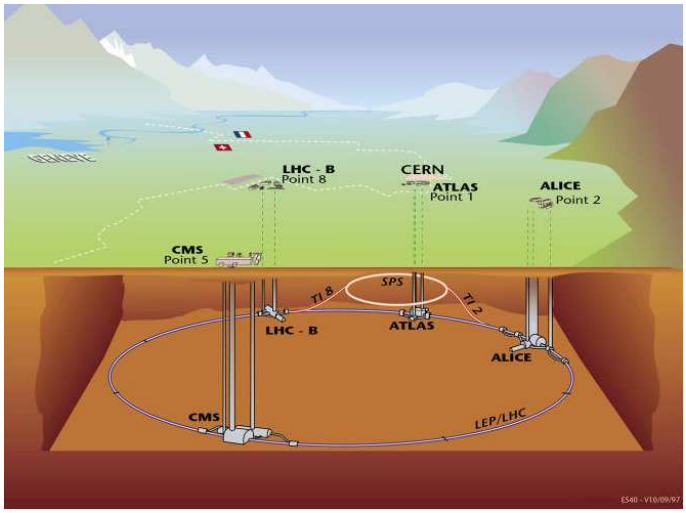

Figure 2.2: The four LHC experiments [12].

The LHC will accelerate protons in a first phase and heavy ions at a later stage. In either case, the colliding particles carry the same electric charge, making two separate beam lines necessary to allow the circulation of identically charged particles in opposite directions. These beam lines are crossed at four points of the accelerator ring to permit the collision of protons of the two different beams. Four detectors will be placed at these crossing points, see Figure 2.2:

- ALICE (A Large Ion Collider Experiment) will examine heavy ion (Pb-Pb) collisions with center of mass energies up to $1250\,TeV$ [13].
- LHCb (LHC beauty experiment) will focus on the effect of CP[2] violation in the decay of bottom quarks [14].
- CMS (Compact Muon Solenoid) and ATLAS (A Toroidal LHC ApparatuS) are two general purpose detectors located in opposite straight sections, [15] and [16].

In order to keep the high energy protons ($v = 99.9999991\%\,c$, with c denoting the speed of light) on track, 1296 large superconducting dipole magnets, cooled down to $1.9\,K$ with liquid helium, must be installed [17]. Their magnetic field strength will reach 8.33 Tesla. A cross-section of such a dipole magnet setup surrounding both beam lines is shown in Figure 2.3.
Additionally, 6.9 Tesla superconductive quadrupole magnets will be necessary to focus the proton beams. The LHC can accelerate protons up to an energy of $7\,TeV$ resulting in a center of mass energy of $\sqrt{s} = 14\,TeV$. This allows a search for new particles with masses up to about $5\,TeV$ (*cf.* Section 1.1.3). The interaction interval separating two proton bunches was set to $24.95\,ns$, corresponding to a bunch crossing frequency slightly above $40\,MHz$. As already shown in Section 1.1.3, cross-sections for the direct production of

[2]Charge conjugation and Parity.

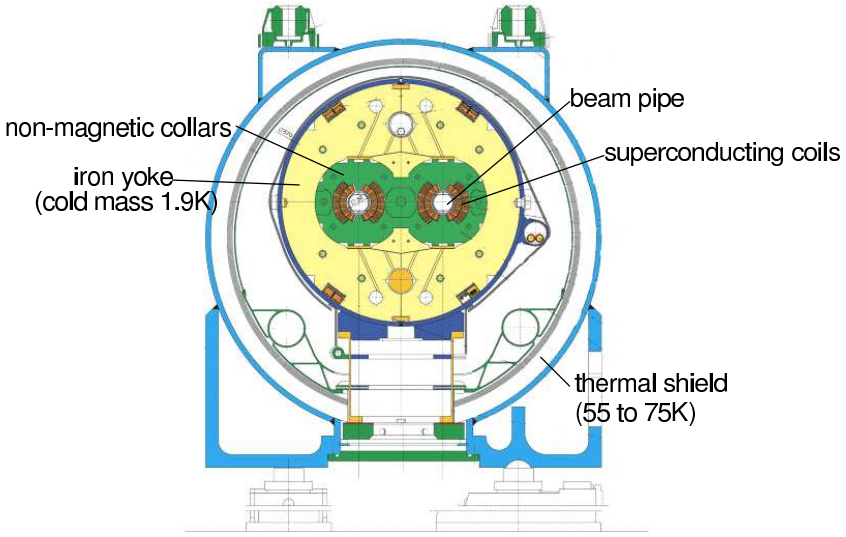

Figure 2.3: Cross-section of a LHC two-in-one dipole [18].

heavy particles like the proposed Higgs boson are extremely small (*cf.* Figure 1.3). Thus, it is indispensable to reach a high luminosity[3] in order to produce a sufficient amount of the rare deep inelastic scattering events. The luminosity $\mathcal{L}$ of a circular accelerator like the LHC can be calculated using the formula

$$\mathcal{L} = \frac{N_a \cdot N_b \cdot j \cdot v/C}{A}, \tag{2.1}$$

with N_a and N_b being the number of protons in bunches[4] a and b respectively, j the number of bunches in the beam, v the velocity of the protons, C the circumference of the accelerator ring and A the cross-sectional area of the beam [1]. The reaction rate R at a given interaction point is related to the cross-section σ of a particular reaction and the luminosity by

$$R = \sigma \cdot \mathcal{L}. \tag{2.2}$$

Combining the above mentioned construction parameters, it can be concluded that the LHC will be an excellent laboratory for the discovery of new physics. The LHC design luminosity is $10^{33}\,cm^{-2}s^{-1}$ at the beginning of operations and even $10^{34}\,cm^{-2}s^{-1}$ at a later stage. The LHC will surpass the luminosity of the Tevatron at Fermilab, which currently is the collider with the highest center of mass energy ($\sqrt{s} = 1.8\,TeV$), by a factor of 100. Therefore, it is expected to observe about 25 proton-proton collisions in every bunch-crossing, *i.e.* every $25\,ns$, assuming a total cross-section of $100\,mb$[5] for proton-proton scattering (*cf.* Figure 1.3 and Equation 2.2).

[3] Luminosity is the number of particles crossing a unit area per unit time.
[4] Each bunch at LHC will contain about 10^{11} protons.
[5] $1\,barn = 1\,b = 10^{-24}\,cm^2$.

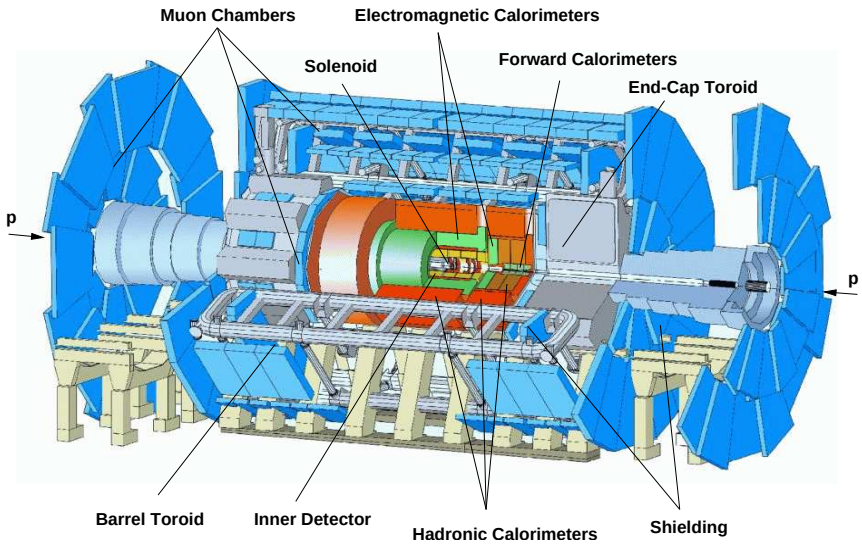

Figure 2.4: The ATLAS detector [19].

2.2 The ATLAS Detector

ATLAS is a general purpose detector dedicated to investigate a broad spectrum of physics accessible with the LHC. The main objectives of ATLAS are the discovery of the presumed Higgs boson and the search for physics beyond the Standard Model. Additionally, ATLAS will be able to probe fundamental Standard Model parameters like the masses of the W boson and the top quark with high accuracy: at a luminosity of $\mathcal{L} = 10^{33}\, cm^{-2} s^{-1}$, $10^7\, t\bar{t}$ quark-antiquark pairs and 3×10^8 W bosons are expected to be produced per year, resulting in an unprecedented amount of available data [20]. Results and measurements from previous experiments, mainly from LEP and Tevatron, will most probably be improved by the data that will be taken at the LHC. More than 2000 physicists from 150 universities and laboratories in 34 countries all over the world participate in the ATLAS collaboration. Each group is responsible for the construction of a subdetector part. An overview of the complete system is shown in Figure 2.4. The detector dimensions are considerable: its length is $40\, m$, its radius amounts to $10\, m$, which is comparable to a five story building, and ATLAS' weight will be about $7000\, t$.
Adapted to the spherical symmetry of the detector, spherical coordinates with the origin at the interaction point in the center of the detector were chosen to describe each point in space. The z-axis corresponds to the beam axis, the azimuthal angle ϕ is the angle around the beam axis in the plane perpendicular to the z-axis, while the polar angle θ is measured from the beam axis. For reasons of convenience, it is common to replace the polar angle θ by the pseudorapidity η. Pseudorapidity is related to the polar angle by

$$\eta = -\ln \tan \frac{\theta}{2}, \tag{2.3}$$

differences in η having the advantage of being Lorentz invariant. The following sections give a brief summary of the ATLAS subdetectors indicated in Figure 2.4, starting from the

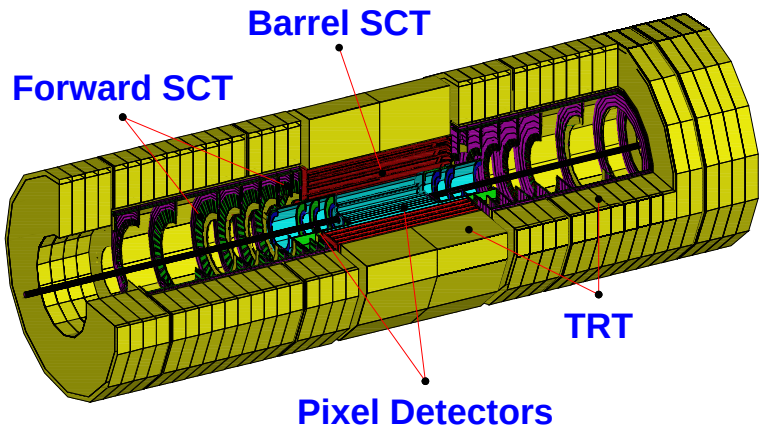

Figure 2.5: The Inner Detector of the ATLAS experiment [21].

interaction point: the inner detector, the calorimeter, and the muon spectrometer. Special attention will be paid to the calorimetric system which constitutes the signal provider for the Level-1 Calorimeter Trigger. More details on the detector can be found in [20].

2.2.1 The Inner Detector

Having a diameter of $3.3\,m$ and a length of $7\,m$, the cylindrically shaped inner detector is located around the interaction region. A layout of the subdetector is shown in Figure 2.5. Its task is to reconstruct tracks of charged particles and interaction vertices with very high spatial resolution. The inner detector is enclosed by a $2\,T$ superconducting solenoid[6] that deflects charged particles and hereby separates their tracks, allowing charge and momentum measurements by calculating the curvature of the tracks. Lying closest to the point of the proton-proton collision, pixel detectors are the most precise detectors to pinpoint a particle's location, reaching a spatial resolution of $14\,\mu m$. This is necessary in order to separate hundreds of tracks produced by a high energy proton-proton collision in ATLAS and to decide whether a track originates from the primary interaction point or from a decay process following the actual collision. The next layer of the inner detector are the silicon microstrip detectors (Barrel SCT[7] and Forward SCT), having an inferior resolution than the pixel detectors. This is acceptable since the track density diminishes with increasing distance from the point of interaction. The Transition Radiation Tracker (TRT), with a resolution of $0.15\,mm$, forms the outer layer of the inner detector: it is a straw tube drift chamber, the tubes having a wire in their center surrounded by an appropriate mixture of gases for particle identification, in this case consisting of 70% xenon, 20% CF_4, and 10% CO_2. Altogether, the inner detector covers pseudorapidity in the range from $\eta = -2.5$ to $\eta = 2.5$.

[6] The magnetic field lines run parallel to the beam axis.
[7] SemiConductor Tracker.

2.2.2 The Calorimeter

Dedicated to measure energy deposits, the next subdetector is the ATLAS calorimeter shown in Figure 2.6. Due to its shape, the cylindrical part is referred to as "barrel", whereas the "lids" of the imagined overturned barrel are called "end-caps". The zone near the beam at both ends of the barrel is named "forward region". The calorimeter can be divided into two subsystems: the electromagnetic calorimeter forms the inner part, while the hadronic calorimeter constitutes the outer part. The calorimetric system plays a crucial role for the whole experiment, since interesting processes, *e.g.* the decay channels of the Higgs boson, are calorimetrically detectable in form of *i.e.* isolated leptons and photons, hadronic jets, high or missing transverse momentum and missing transverse energy E_T^{miss}. The calorimeter covers the region from $\eta = -4.9$ to $\eta = +4.9$ needed for a precise measurement of E_T^{miss}. An example for the importance of the E_T^{miss} measurement is the presumed Higgs decay channel $H \rightarrow WW \rightarrow l\,\nu\,jet\,jet$, which is a dominant decay channel for a Higgs boson with a mass in the range $160\,GeV/c^2 \leq m_H \leq 1000\,GeV/c^2$. To identify this process, one would look for signatures like:

- one lepton and large E_T^{miss},
- two jets with invariant mass of the reconstructed dijet $m_{jet\,jet} \approx m_W$,
- two jets in forward/backward direction.

Technically, the calorimeters are realized by alternating sensitive and absorbing layers (sampling calorimeters). In this way, the detected particles lose energy in the absorbing material by creating secondary particle showers which are then detected in the sensitive layers. In order to localize a signal within the detector, the calorimeter was subdivided into numerous cells or channels (about 200,000 for the electromagnetic calorimeter).

The Electromagnetic Calorimeter

Designed to detect electrons and photons and to measure their energy, the electromagnetic calorimeter consists of alternating layers of liquid argon as sensitive material, and layers of lead as the absorbing material. As the plates of lead are bent into an "accordion" shape, the electromagnetic calorimeter is termed EM Accordion Calorimeter in Figure 2.6. Liquid argon is chosen as sensitive medium because of its insulating properties, its good resistance against high radiation which occurs during beam operation, and its low probability to capture free electrons passing the calorimeter. The latter is indispensable for a reliable energy measurement of the electrons and photons [16]. Lead is chosen as the absorbing material, since it shows a high cross-section for bremsstrahlung and pair production, the two main processes for crossing electrons and photons to lose energy in the absorbing medium. The secondary particle showers produced by these processes excite or ionize atoms in the liquid argon which cause an ionization cascade within the sensitive medium. A dedicated pulse shaper then amplifies and transforms the measured ionization into an electric signal which is then processed. Each signal amplitude is proportional to the energy deposit of the particle shower in the liquid argon of the specific cell. In order to ensure

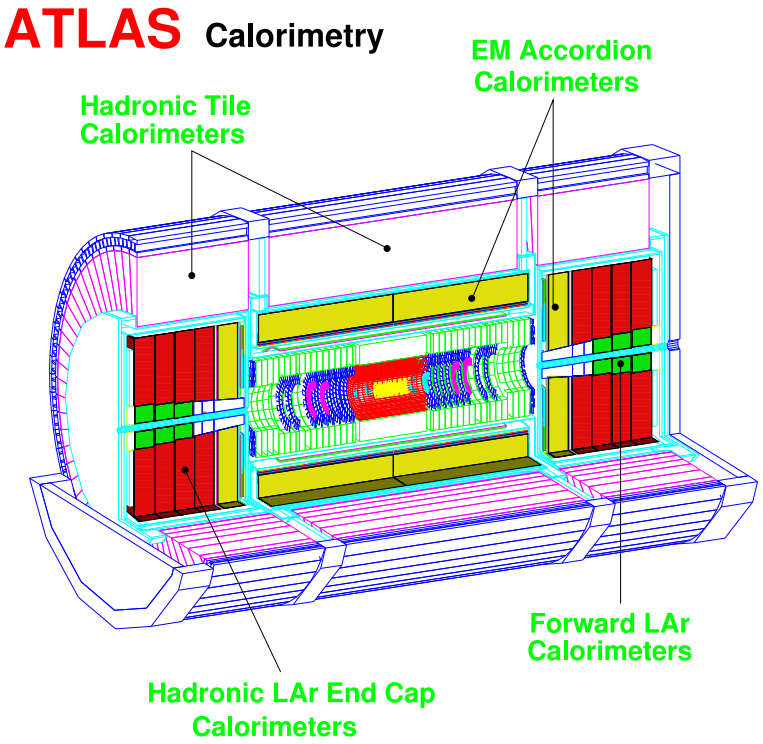

Figure 2.6: The ATLAS Calorimetry [19].

that even very high energy electrons and photons lose most of their energy within the electromagnetic calorimeter, a calorimeter thickness of $\sim 24\,X_0$[8] was chosen for the barrel and $\sim 26\,X_0$ in the end-cap sections (*cf.* Figure 2.6).

The Hadronic Calorimeter

Due to their higher masses, hadrons pass the electromagnetic calorimeter without considerable loss of energy. A hadronic calorimeter therefore enfolds the previously described detector components. Again, liquid argon is used as sensitive material in the forward region detector named Hadronic End Cap (HEC) calorimeter. For the hadronic tile calorimeter, however, scintillating plates of plastic are deployed. Iron (barrel), copper (end-caps) and tungsten (forward region) serve as absorbing materials: as in the electromagnetic calorimeter, the passing particles produce showers of secondary particles. However, the predominant creation process of secondary particles in the case of hadrons is the strong interaction between the crossing particles and the absorber nuclei. Other differences between the two calorimetric systems are the shower expansion and the diversity of the created particles: electromagnetic showers are smaller in transverse direction and consist primarily of electrons and photons whereas the hadronic showers are less confined and additionally more diverse in composition, although pions and kaons outnumber other hadrons.

[8] The radiation length X_0 is the absorber thickness over which the electron or photon energy is reduced by a factor $1/e$.

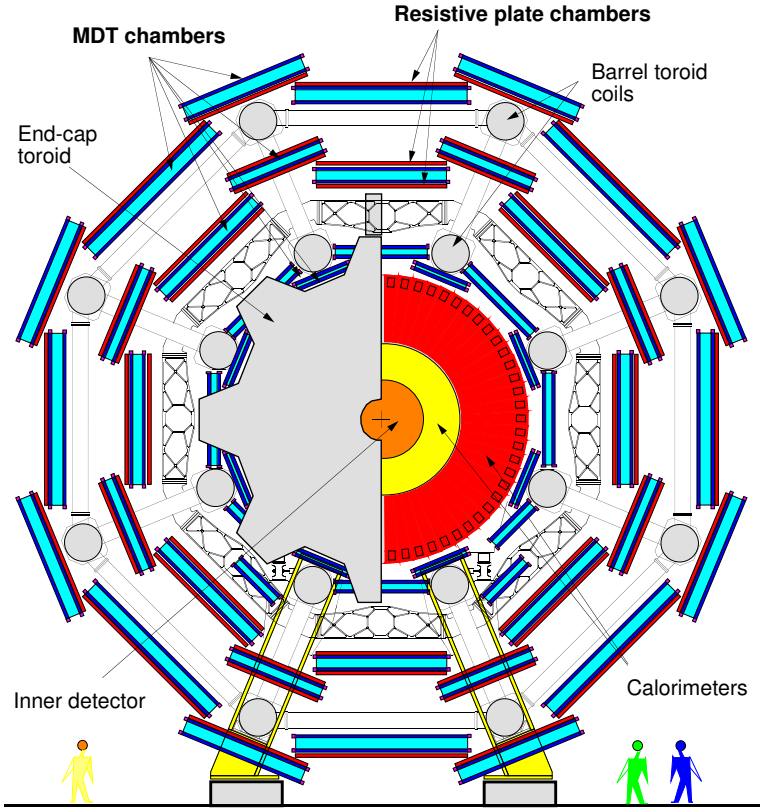

Figure 2.7: Cross-sectional view of the ATLAS muon spectrometer [22].

2.2.3 The Muon Spectrometer

Muons are the only particles that leave a trace in all previously introduced detectors yet passing them almost unhindered. Therefore, the muon spectrometer that surrounds the whole calorimetry provides muon identification. An overview of the Muon Spectrometer is shown in Figure 2.7. Superconducting magnets generate a strong toroidal[9] magnetic field within the spectrometer, forcing charged muons on curved tracks which can be analyzed resulting in a measurement of the muon charge and momentum.
Close to the beam, Cathode Strip Chambers (CSC) are used whereas Monitored Drift Tubes (MDT) are placed in regions of lesser radiative background. Additionally, Thin Gap Chambers (TGC) and Resistive Plate Chambers (RPC) are embedded in the barrel and end-cap regions, respectively, in order to enable the rapid muon tagging needed to identify physically interesting processes like the Higgs decay $H \rightarrow ZZ^* \rightarrow 4\,\mu$ in real-time. For this reason, the fast identification of muons is of crucial importance for the trigger system described in the following chapter.

[9]The magnetic field lines form concentric circles in the plane perpendicular to the beam axis.

Chapter 3

The ATLAS Trigger System

Due to the amount of approximately 147 million readout channels and an interaction rate of about $10^9\,Hz$ at a luminosity of $10^{34}\,cm^{-2}s^{-1}$, huge data sets are produced in each bunch-crossing: Table 3.1 lists the number of read-out channels per subdetector and the respective amount of produced data in each event.

Subdetector	**Number of channels**	**Amount of data [KByte]**
Pixel detector	1.4×10^8	50
Tracker	5.6×10^6	850
Calorimeter	2.3×10^5	180
Muon spectrometer	1.3×10^6	200
Total	147.13×10^6	1280

Table 3.1: Amount of data produced in the various ATLAS subdetectors in every bunch-crossing [16].

As one can see, a total of 1.28 MByte is produced every $25\,ns$, corresponding to a data rate of 51.2 TByte/s. Since it is impossible to store all data for further off-line analysis, a multi-level online trigger system was designed to reduce the data rate from the initial $40\,MHz$ LHC bunch-crossing frequency to an manageable data rate of about $100\,Hz$.

3.1 Overview of the Trigger Concept

In order to achieve the required rate reduction factor of about 10^7, a three level trigger system was proposed, consisting of the Level-1 Trigger, the Level-2 Trigger, and finally the Event Filter. Of course, all events containing processes of physical interest have to be included in the data sets that are actually written onto permanent storage media. Each trigger level reduces the data rate by rejecting events which do not fulfill its selection criteria. A schematic overview of the data flow is shown in Figure 3.1.
One of the main characteristics of a trigger is the time interval needed to decide whether or not an event is accepted. This period is referred to as trigger latency. Ideally, the latency should be smaller than the time between two bunch-crossings. However, in the

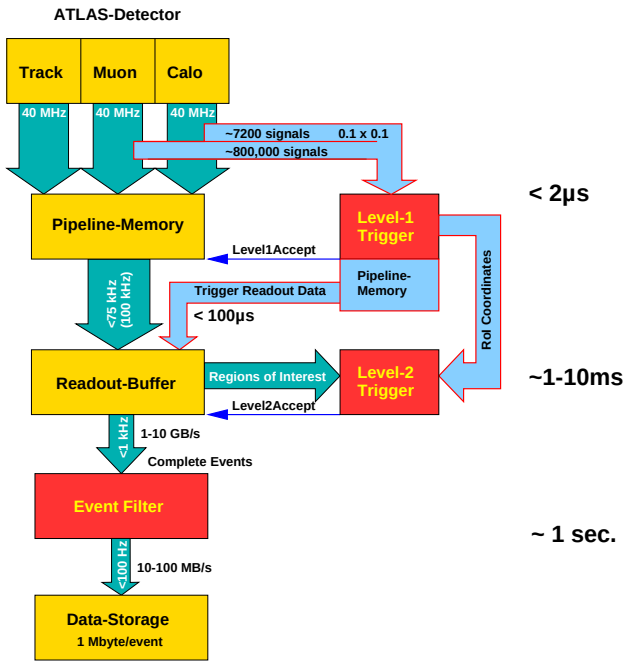

Figure 3.1: Detector read-out and trigger system [12].

case of the LHC, this period of time is too short since it takes about one second to fully reconstruct an event. Therefore, all data collected by the different subdetectors need to be temporarily stored (buffered) in a pipeline memory. In the case of the Level-1 Trigger, the maximum allowed latency amounts to $2\,\mu s$, which is equal to about 80 bunch-crossings. This is a compromise between pipeline length, which is limited primarily for financial reasons, and the time needed to evaluate the data as thoroughly as possible. Therefore, the Level-1 Trigger decision relies on reduced calorimeter granularity and data coming from the fast RPC and TGC muon chambers mentioned in Section 2.2.3. No data from the inner detector can be taken into account for the Level-1 decision (*cf.* Section 2.2.1). The Level-1 Trigger reduces the event rate to below $100\,kHz$.
Following a Level-1 Accept, the Read-Out Buffers (ROBs) store all detector data from the selected event until the Level-2 Trigger reaches its decision. At that point, the data are discarded if Level-2 rejects the event or processed further to the event filter in the case of a Level-2 Accept. Due to a latency of about $10\,ms$, the Level-2 Trigger investigates not all data in the ROBs but only the Regions Of Interest[1] (ROI) directly provided by the Level-1 Trigger. This second decision process reduces the event rate to below $1\,kHz$.
After a Level-2 Accept, the event filter selects the bunch-crossing data that are stored permanently for off-line analysis at a later stage. Again, all rejected data are discarded. The event filter reconstructs the whole event in full granularity and resolution. It employs algorithms similar to those used later in off-line analysis such as cluster and jet reconstruction algorithms. The event builder reduces the data rate to about 100 MByte/s, corresponding to about 100 accepted events per second.

[1]Regions Of Interest are detector coordinates in η and ϕ which contain interesting event signatures.

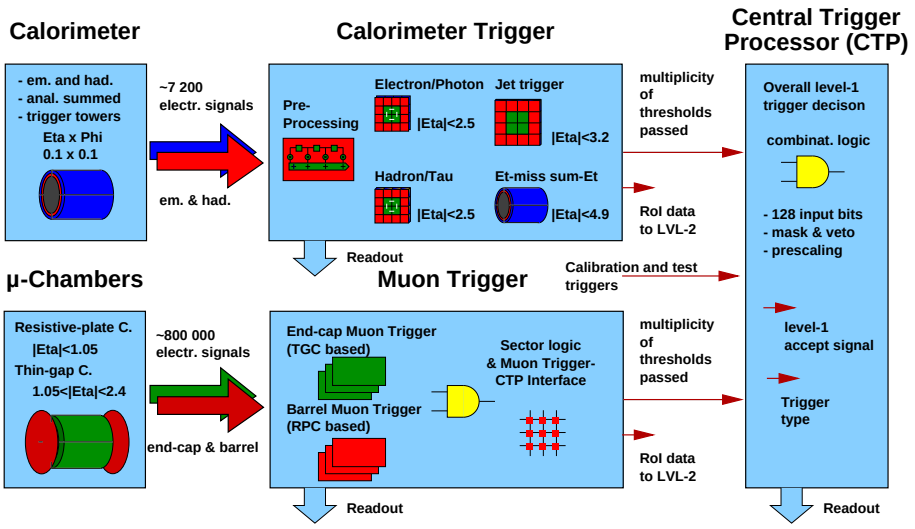

Figure 3.2: The ATLAS Level-1 Trigger system with its major components: the Calorimeter Trigger, the Muon Trigger, and the Central Trigger Processor [12].

3.2 The Level-1 Trigger

The Level-1 Trigger system consists of three major building blocks: the Central Trigger Processor (CTP), the Muon Trigger subsystem, and the Calorimeter Trigger subsystem. A schematic overview of the Level-1 Trigger system is shown in Figure 3.2.

The Level-1 Trigger reaches its decision by applying various algorithms that search for isolated electrons and isolated photons, hadrons and taus, jets and muons. In addition, the calculation of the total energy deposit in the calorimeter allows an estimate of the missing transverse energy E_T^{miss} needed for the identification of decays involving almost non-interacting particles such as neutrinos. These interactions are particularly interesting since some promising Higgs boson decay channels comprise neutrinos (*cf.* Section 2.2.2). Since the Level-1 Trigger latency has to be less than $2\,\mu s$, all trigger algorithms are implemented in dedicated hardware, both Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs). Therefore, the Level-1 Trigger is referred to as "hardware trigger". Since this thesis deals with a test system for the Level-1 Calorimeter Trigger, it will be described in detail in Section 3.3.

The Level-1 Muon Trigger receives data only from a subset of muon detectors, namely the RPC and TGC chambers introduced in Section 2.2.3. About 800,000 trigger channels form the input of the Muon Trigger. As a result, ROIs are sent to the Level-2 Trigger system with every positive trigger decision.

The task of the Central Trigger Processor is to combine the information of both Calorimeter Trigger and Muon Trigger to make a decision for the whole Level-1 Trigger system. An overall Level-1 Accept signal representing this decision is generated and sent to readout and front-end systems along with the corresponding bunch-crossing and event number.

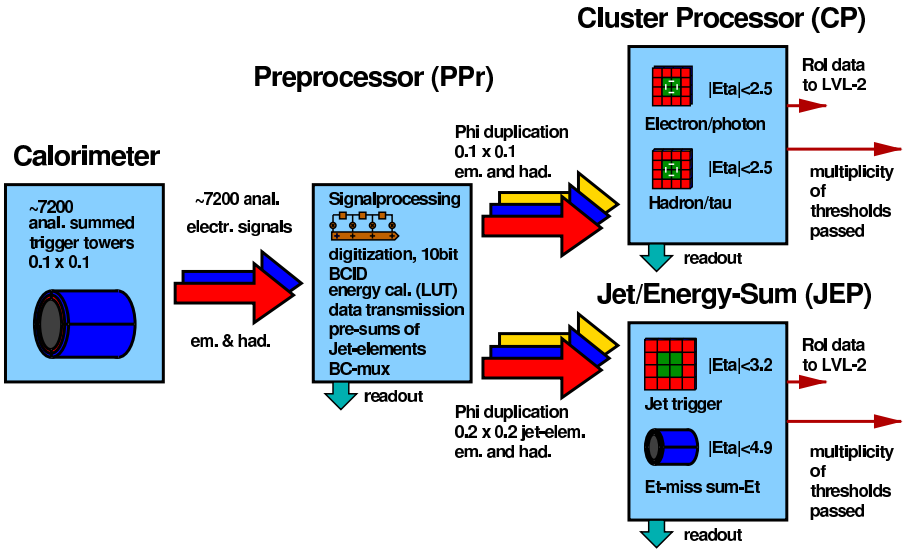

Figure 3.3: The calorimeter trigger with its three processors: the Pre-Processor, the Cluster Processor and the Jet/Energy-Sum Processor [12].

3.3 The Calorimeter Trigger

Figure 3.3 illustrates the structure of the ATLAS Level-1 Calorimeter Trigger. It processes about 7300 trigger tower signals, which are obtained by summing up as much as 60 calorimeter channels. Each trigger tower signal represents the energy deposit within a cell of 0.1×0.1 in η and ϕ direction, respectively. The depth of the cell is given by the depth of the electromagnetic or hadronic calorimeter at a given point of the calorimeter. After passing a series of operational amplifiers, pulse shapers, buffers, time delay circuits, and adding circuits, the trigger tower signals are transmitted through $60\,m$ long twisted pair cables[2] [16]. The receiver stations perform a first calculation to determine the transverse energy deposit. Then, the analog pulses reach the Pre-Processor – which forms the first part of the Calorimeter Trigger – where they are initially digitized. Following this procedure, the transverse energy is fine-calibrated and the pulse is assigned to the correct bunch-crossing (bunch-crossing identification, BCID). The latter is necessary, for the pulse extends over several bunch-crossing periods. A detailed description of the Pre-Processor is given in Chapter 4. The digital data are then sent to the subsequent processors which work in parallel:

1. The Cluster Processor uses an electron/photon and a hadron/tau algorithm to identify isolated particles. This is achieved by first comparing the energy deposit in an electromagnetic or hadronic calorimeter trigger tower cell, respectively, with a given and programmable threshold. The isolation criterion is checked by comparing the energy deposit in the primary trigger tower cell with that in the adjacent cells. If

[2]Twisted pair cables consist of two equally long twisted cables. They are well suited for transmitting differential signals while minimizing the picking-up of electromagnetic noise.

these neighboring signals fall below another programmable threshold, the isolation criterion is met. The distinction between an electron/photon or a hadron/tau is done by checking the hadronic cell lying behind (with respect to the point of interaction) the primary cell in the case of an electron/photon, and by checking the electromagnetic cell lying before the primary cell in the case of a hadron/tau. For the former, the energy deposit is expected to be small in the hadronic cell, whereas there should be an energy deposit in both the hadronic and the electromagnetic cells for hadrons and taus since they produce particle showers in both calorimeters.

2. The Jet/Energy-Sum Processor identifies jets and ascertains the total transverse energy E_T^{tot} as well as the missing transverse energy E_T^{miss}. Since jets are objects that can extend over several trigger tower cells, the jet algorithm is applied to a quadratic area of trigger towers. This pattern is then moved along the surrounding trigger tower cells and the included energy deposit is summed up. Whenever one out of eight programmable thresholds is exceeded, a jet of the surpassed threshold energy is recorded. The programmable size of the selection pattern is crucial to an algorithm, since a pattern which is too small would lead to underestimation of the jet energy, whereas a pattern that is too large would result in overestimating the jet energy. The E_T^{miss} algorithm sums up all measured transverse energies from all trigger towers and from this calculates the missing transverse energy. A large acceptance range of $-4.9 < \eta < +4.9$ is mandatory for the E_T^{miss} algorithm to minimize mistakes from excluding jets that lie outside of the specified range.

All mentioned trigger algorithms, therefore, identify so-called trigger objects by measuring the transverse energy deposit in the trigger tower cells. The amount of trigger objects, along with the exceeded threshold, is passed on as "multiplicity" to the Central Trigger Processor. In the case of a Level-1 Accept, the coordinates of the object are sent to the Level-2 Trigger system as a ROI.

Chapter 4

The Level-1 Calorimeter Trigger Pre-Processor

In the previous chapter, the ATLAS Level-1 Trigger with its three main data processing units – the Pre-Processor, the Cluster Processor, and the Jet/Energy-Sum Processor – was introduced. This chapter focuses on the Pre-Processor which is currently being developed at the Kirchhoff-Institut für Physik.

4.1 Overview of the Pre-Processor System

The task of the Pre-Processor system is to receive the 7296 analog calorimeter trigger tower signals, digitize them, perform complex digital signal processing such as bunch-crossing identification (BCID), and finally to create two independent data streams: the real-time data path provides digital data to the subsequent Cluster and Jet/Energy-Sum Processors whereas the bidirectional ReadOUT data path is used for the configuration of the Pre-Processor and the readout of trigger data without trigger dead time. The ReadOUT data allow a check of the overall trigger performance without restricting the real-time data acquisition. More precisely, the two Pre-Processor tasks consist of the following:

Preprocessing

- Reception of differential analog trigger tower signals including the conversion into unipolar signals and a zero baseline adjustment for each input signal.
- Digitization of analog trigger tower signals with 10-bit resolution
- Signal phase adjustment and LHC clock synchronization is necessary because of varying time-of-flight delays for the different channels
- Bunch-crossing identification is needed to assign the transverse energy deposition to the correct bunch-crossing

- Energy calibration: a Look-Up Table (LUT) is used to fine-calibrate the digitized data to the deposited transverse energy E_T. It maps the 10-bit data to 8-bit with a Least Significant Bit (LSB) of $1\,GeV$

- Formation of Jet Elements: four 8-bit trigger towers are pre-summed to Jet Elements. This is done separately for the electromagnetic and hadronic calorimeters to allow possible different jet thresholds in the Jet/Energy-Sum Processor

- Serial data transmission to the subsequent Cluster and Jet/Energy-Sum Processors

ReadOUT

- Readout of raw and preprocessed trigger data allows a check of the overall trigger performance

- Histogramming includes the possibility to monitor the calibrated output of the system right after the LUTs

More details regarding these tasks are given in the following section. Overall, the full Pre-Processor system will consist of 128 identical Pre-Processor Modules (PPMs). The data produced by these PPMs are collected by 16 Readout Driver Modules (RODs) using the circular pipeline bus architecture [23] shown in Figure 4.1. S-Links, (CERN Standard Links [24]) transfer the data into the Read-Out Buffers if requested by a Level-1 Accept signal. All mentioned modules will be installed in 8 crates altogether. Each crate will be provided with a VMEbus[1] [25] crate controller to enable VME access to the different modules.

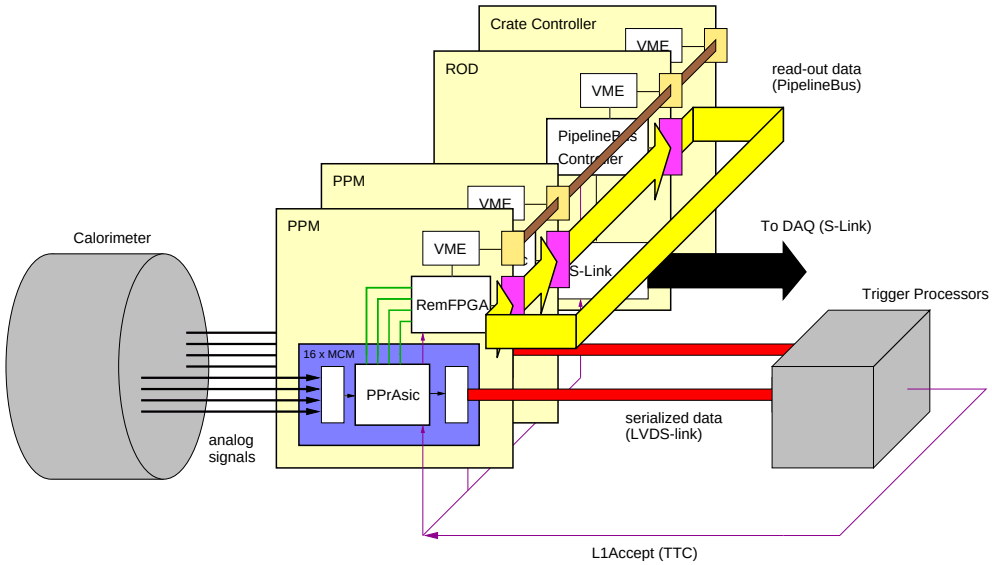

Figure 4.1: Block diagram of the readout configuration [23].

[1] Versa Module Eurocard.

As stated in Chapter 3, the latency for the entire Level-1 Trigger is $2\,\mu s$. For the Pre-Processor however, only $0.45\,\mu s$ or 18 bunch-crossings are allowed to perform the above mentioned tasks since it constitutes only a part of the Level-1 trigger architecture. This results in the need for a fast system with high integration density to minimize signal run time.

4.2 Hardware Components of the Pre-Processor Module

Each of the 128 PPMs receives and processes 64 trigger tower signals [26]. Figure 4.2 shows a layout of the PPM, which will be a Printed Circuit Board (PCB) that is 9U[2] high and $40\,cm$ deep. Four connectors at the front (on the left hand side of Figure 4.2) of the PPM each receive 16 differential trigger tower signals. Four Analog Input Boards then pre-format the signals for the following main component of the PPM: the 16 Pre-Processor Multi-Chip Modules (PPrMCMs[3]) which process four analog signals each. The positioning of the MCMs has been optimized with respect to guaranteeing good heat exchange and minimizing crosstalk between the analog inputs and the high speed differential outputs. Temperature simulations of different MCM arrangements were carried out in [27].

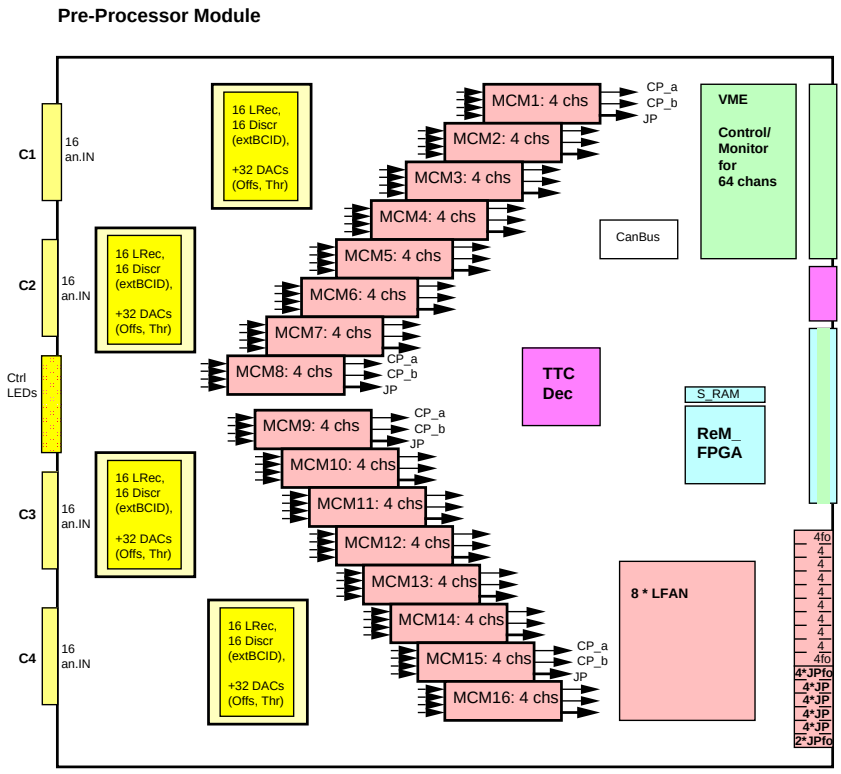

Figure 4.2: Layout of the Pre-Processor Module (PPM) [28].

[2]U stands for Unit, used in VME specifications. $9\mathrm{U} = 36.6\,cm$.
[3]In the following, the PPrMCM will be referred to as MCM.

The MCMs produce the already introduced independent data streams: the ReadOUT data are received by the RemFPGA[4] which sends them on to the pipeline bus on the back of the PPM. The real-time data, however, are sent to driver chips located in the lower right corner of the Figure 4.2. These data are then transmitted to the Cluster and Jet/Energy-Sum Processors via $10\,m$ cables [28]. On the final board, either FPGAs or ASICs will be used as driving chips. More precisely, a candidate for the former chip type is the Virtex-E 50 by Xilinx. This commercial chip is capable of transmitting data differentially by using the LVDS[5] format. An alternative is the implementation of the LFAN[6] ASIC that has already been tested successfully [29]. Another PPM component is the CanBus [30] used for monitoring purposes like the readout of temperatures and supply voltages of the MCMs. The TTC[7] daughterboard receives signals global to the experiment, *e.g.* a Level-1 Accept signal or the $40\,MHz$ LHC bunch-crossing clock, and distributes it to the other PPM components.

4.2.1 The Analog Input Board

Four Analog Input Boards are plugged onto each PPM as daughterboards. Every board processes 16 trigger tower signals. A front and back view of the Analog Input Board is shown in Figure 4.3.

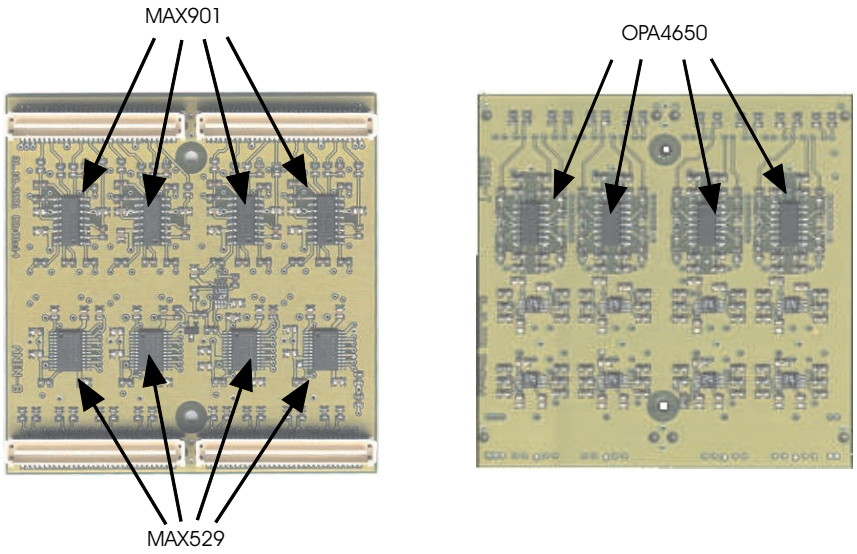

Figure 4.3: Photograph of the Analog Input Board.

First, the differential input signals are converted to single-line signals by the operational amplifier OPA4650 [31]. The input voltage is mapped to an interval ranging from 0 to $2.5\,V$, corresponding to a transverse energy range of 0 to $250\,GeV$. The next operational

[4]Readout Merger Field Programmable Gate Array.
[5]Low Voltage Differential Signaling.
[6]LVDS Fanout.
[7]Trigger and Timing Control system.

amplifier, the LT1813 [32], reduces the signal voltage to $1.0\,V_{pp}$[8] in order for the signal to meet the requirements of the Analog-to-Digital Converters (ADCs) on the MCM (*cf.* Section 4.2.2). Additionally, eightfold MAX529 Digital-to-Analog Converters (DACs) [33] allow a shifting of the zero line for each signal. Besides these signal formatting tasks, the Analog Input Boards generate the so-called "external BCID" signal: since the pulses created in the calorimeter extend over several bunch crossings, it is necessary to determine the pulse maximum and to perform a BCID. The external BCID is produced by the comparator MAX901 [34]. If the single line signal exceeds a programmable threshold, the comparator generates a "1", and else outputs a "0". All DAC and comparator settings can be programmed using the SPI[9] explained in Section 6.2. Besides the type of BCID described above, two further algorithms are applied to the data to determine the correct bunch crossing. Both are implemented in the Pre-Processor ASIC described in the following section.

4.2.2 The Pre-Processor Multi-Chip Module

The main functionalities of the PPM are implemented in the 16 MCMs: they digitize the incoming analog trigger tower signals, perform BCID and calibration algorithms, and produce the two data streams introduced in Section 4.1. Nine dies[10] are placed on each MCM: four ADCs, three LVDS serializers, a Phos4, and a Pre-Processor ASIC (PPrASIC). The former seven dies are commercial chips, whereas the latter two are ASICs developed by the CERN Microelectronics Group [35] and the ATLAS group at the Kirchhoff-Institut [36] respectively. Figure 4.4 shows a photograph of a fully assembled MCM.

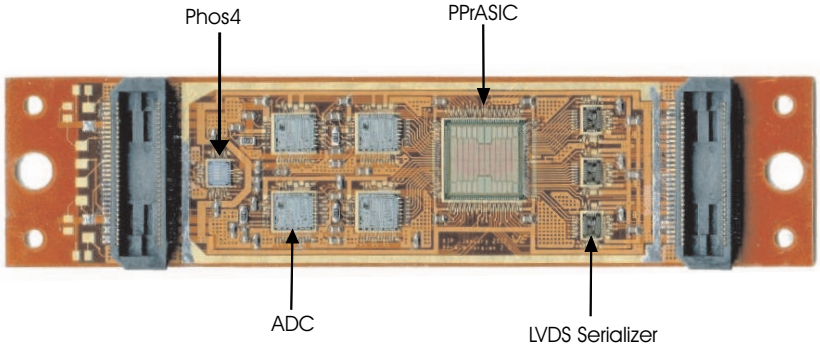

Figure 4.4: Photograph of the Pre-Processor Multi-Chip Module (MCM) [37].

A block diagram illustrating the data path of each trigger tower signal through the MCM is shown in Figure 4.5. In the following, the signal processing pathway through a MCM will be referred to as "channel".
As a first step, the incoming signals are digitized with a sampling rate of $40\,MHz$. Four AD9042 ADCs by Analog Devices [38] assume this task. The input voltage ranges from

[8] $1\,V$ peak-to-peak.
[9] Serial Peripheral Interface.
[10] A die is a chip without the packaging around it.

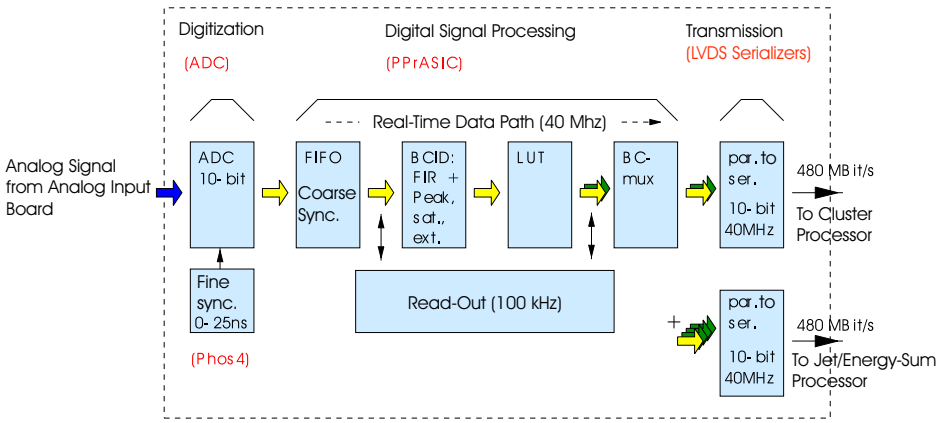

Figure 4.5: Block diagram of the signal processing within the MCM [37].

$1.9\,V$ to $2.9\,V$ based on the internal reference voltage of $2.4\,V$. These ADCs are able to digitize data with a 12-bit resolution. However, the two LSBs are left unused. The resulting 10-bit digitization range from 0 to 1023 and an input voltage of $1\,V_{pp}$ corresponding to a LSB of about $1\,mV$ is satisfactory for the intended purpose. To ensure that every trigger tower signal is sampled at its maximum, the ADC sampling time of the trigger tower signals can be adjusted independently for each channel within a range of $25\,ns$ in steps of $1\,ns$. This is realized by using the Phos4 ASIC [35]. A 10-bit wide data bus then transfers the digitized data from each ADC to the PPrASIC which handles all four channels on a MCM and performs all digital data processing. A detailed description of the PPrASIC is given at a later stage in this section.

The real-time outputs of the PPrASIC are connected to three National Semiconductors DS92LV1021 LVDS serializers [39] via a 10-bit wide data bus for each serializer. Serializing the data is mandatory, for a parallel transmission to the following Cluster and Jet/Energy-Sum Processors exceeds the acceptable number of cables. The reason why only three LVDS serializers are sufficient to provide full speed real-time data to the parallel working Cluster and Jet/Energy Processors is twofold. First, a 2:1 multiplexing scheme was integrated in the PPrASIC. This bunch-crossing multiplexing (BC-Mux) is applied to the data intended for the Cluster Processor, reducing the number of serializers from four to two. Secondly, four trigger tower signals are merged into a single Jet Element to be sent to the Jet/Energy-Sum Processor. With a clock speed of $40\,MHz$, this results in a data rate of 400 Mbit/s, or 480 Mbit/s if the START and STOP bits that are sent before and after each 10-bit LVDS data word are included. A 10-bit LVDS data word sent to the Cluster Processor therefore consists of an 8-bit energy value, a bunch-crossing multiplexing status bit, and a parity bit which is used for debugging purposes. In the case of the Jet/Energy-Sum Processor, the 10-bit LVDS data word is either composed of a 9-bit energy value and a parity bit – again intended for error diagnostics – or of a 10-bit energy value depending on the setting of the PPrASIC.

The ReadOUT data path will be introduced in the following section. A more thorough description of the Pre-Processor MCM including details on mass production and testing plans is given in [37].

The Pre-Processor ASIC

The Pre-Processor ASIC constitutes the central component of the MCM. It conducts all digital data processing tasks shown in Figure 4.5. The processing involves synchronization of channels using FIFOs[11], BCID, calibration through LUTs, generation of Jet Elements, and BC-Mux. These tasks will be briefly introduced in this section; more specific documentation on the PPrASIC can be found in [36].
The Pre-Processor ASIC is a digital chip designed using the hardware description language Verilog[12] [40]. After conscientious simulations the chip was submitted for production in January 2002. The chip was manufactured using a $0.6\,\mu m$ CMOS[13] process offered by Austria Micro Systems (AMS) [41]. The PPrASIC consists of about 990,000 transistors and 8.125 KByte RAM[14]. The chip area is $68.89\,mm^2$. Figure 4.6 shows the layout and a photograph of the actual chip: the four colors in the layout represent the area where the logic for each of the four channels is placed. The 24 rectangles denote the chips RAM blocks.

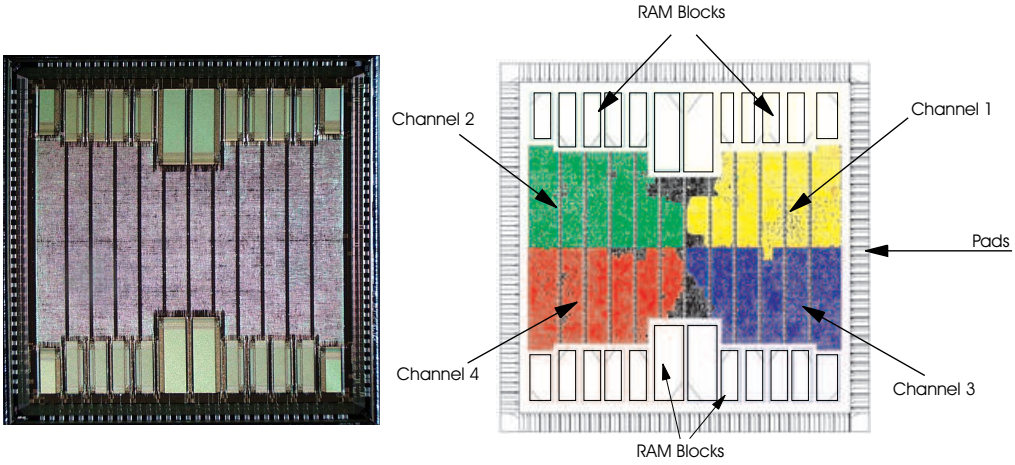

Figure 4.6: Photograph and Layout of the Pre-Processor ASIC (PPrASIC) [36].

By default setting, all data arriving from the ADCs are latched into the PPrASIC using the rising edge of the LHC clock. The alternative use of the falling edge is also implemented in the PPrASIC. Because of time-of-flight differences of the particles from the point of interaction to the various trigger towers, the incoming signals have to be synchronized to the same bunch crossing. Another reason for the need of synchronization are the different cable lengths that result from the varying distances between the trigger towers and the trigger electronics. The coarse synchronization, in steps of $25\,ns$, is done by FIFOs which store the digital data as long as necessary to compensate for the mentioned varying time delays. The fine tuning in steps of $1\,ns$ is achieved by the Phos4 chip. This ensures that the signal can always be sampled "on peak".

[11] First-In-First-Out.
[12] Verifying Logic.
[13] Complementary Metal Oxide Semiconductor.
[14] Random Access Memory.

Two BCID algorithms are implemented in the PPrASIC: one is optimized for saturated pulses, the other for pulses below the saturation level. The latter is composed of the FIR[15] Filter and a peak-finder algorithm. Both BCID algorithms work in parallel and are always active. As mentioned in Section 4.2.1, a third mechanism is used to perform the bunch crossing identification: the external BCID generated by the Analog Input Board. A decision logic in the PPrASIC maps these three BCID algorithms onto three disjoint energy intervals. The interval limits are set by two externally programmable energy thresholds. A LUT is associated with each energy interval, determining which BCID algorithm is going to be used for that specific energy interval. The possible working range of the three BCID algorithms overlap in large areas, resulting in a good flexibility of the decision process.
Another LUT is used to fine calibrate the 10-bit digital data to a 8-bit measurement of deposited transverse energy. This is done by using a 1024×8 bit memory. Additionally, a constant value (pedestal) can be subtracted from the data and a threshold can be applied to suppress noise.
Jet Elements are produced by summing up four adjacent trigger tower signals. This leads to a Jet Element size of 0.2×0.2 in $\eta \times \phi$. The 10-bit sum of the four 8-bit wide trigger tower signals can be truncated to 9-bit before transmission to the LVDS serializers.
In the case of the data sent to the Cluster Processor, data from two trigger towers are transmitted one after another in two consecutive clock cycles. This is possible, since the next time slot after a BCID signal is empty by definition. A status bit is inserted to distinguish between the two original channels.
Each PPrASIC is equipped with two serial interfaces, also indicated in Figure 4.5. They enable data readout for system diagnostics, namely for trigger decision controlling and detection of malfunctioning channels, as well as access to internal configuration registers of the PPrASIC. However, in the usual data taking process it is planned to read out trigger data only in the case of a Level-1 Accept. This results in an expected readout rate of $100\,kHz$. The first serial interface provides access to the digital data directly after the ADCs. Calibrated data can be read out via the second interface after passing the BCID algorithms and the LUT. In order to allow for a readout of Pre-Processor data without generating trigger dead time, internal pipeline memories store the real-time data. The memory depth amounts to 128 data words, corresponding to $3.2\,\mu s$. With each Level-1 Accept signal, the corresponding data are copied into a Derandomizer Buffer from which they can be read out. A buffer is needed, since the Level-1 Accept rate of $100\,kHz$ is only an average value. Therefore, one needs to compensate for statistical fluctuations of the accept decision rate. The Derandomizer Buffers guarantee a readout of trigger data even at a high statistical accumulation of Level-1 Accepts. Playback Memories are another category of memories implemented in the PPrASIC. They can be used to write data from the serial interfaces into the ASIC for testing purposes.

The Readout Merger FPGA (RemFPGA)

Each PPM carries a RemFPGA (Virtex-E XCV1000 [42]). In the case of a Level-1 Accept signal, the RemFPGA collects readout data from all 32 serial interfaces of the 16 PPrASICs

[15] Finite Impulse Response.

and stores them in internal memory blocks. In order to reduce the data rate for further readout, a compression algorithm is applied to the readout data. The reduction factor is about 2.3 [43]. The pipeline bus shown in Figure 4.1 is used to send data from eight RemFPGAs to the Readout Driver (ROD) which transmits them on to the ATLAS-DAQ[16]. A prototype for the ROD was designed and tested successfully [44]. Additionally, the RemFPGA is responsible for configuring the Phos4 chips on the MCMs as well as the DACs on the Analog Input Boards. These configuration issues will be explained in detail in Chapter 6.

[16]Data AcQuisition System.

Chapter 5

The Pre-Processor Test Environment

As stated in the previous chapter, the Pre-Processor system will consist of 128 Pre-Processor Modules. Therefore, about 3200 MCMs have to be produced. This includes 50% spare MCMs required to keep the trigger system operational over the anticipated running period of ten years. All final MCMs will be assembled by HASEC-Elektronik [45], a commercial electronics company. To allow the testing of the MCMs at the manufacturing company, a portable test system has to be designed. Additionally, a single MCM test has to be rather fast in order to quickly separate working units from faulty ones which then pass through a repairing cycle [37]. A prototype for this test system is described in this chapter.
The test system mainly consists of three components: a signal generator, the MCM Testboard, and a data sink which collects the data. A Matrox G450DH[1] graphics card [46] is used to generate the test signals needed to test the MCMs. Electronic components on the MCM Testboard preformat these signals and send them along to an Analog Input Board mounted on the Testboard. The MCM that is to be tested is also plugged onto the MCM Testboard from which all MCM output is then sent to a set of PCBs installed in a VME crate. Finally, the data can be read out onto permanent storage media via a VMEbus system controlled by the crate controller. These steps will be explained in greater detail in the following sections.

5.1 The Test Signal Generator

A commercial AGP[2] Matrox G450DH graphics card is programmed to generate pulses very similar to the real calorimeter trigger tower signals. These pulses form the input of the MCM Testboard. The G450DH is equipped with two independent output connectors (15 pin SUB-D) usually used for two independent screens. Each connector therefore issues three analog color signals (red, green, and blue) as well as two digital signals (horizontal

[1] G450DualHead.
[2] Accelerated Graphics Port.

and vertical synchronization). The frequency of the horizontal synchronization signal denotes the horizontal scan rate whereas the frequency of the vertical signal is the refresh rate of the whole screen image. This leads to a total of six analog and four digital signals for a single graphics card. Four out of the six analog signals are chosen to act as input signals to the MCM Testboard. The output voltage of each color signal ranges from $0 - 0.7\,V$. The color intensity is directly proportional to the output voltage: black would therefore correspond to $0\,V$ on each color pin, the brightest red is obtained by an output voltage of $0.7\,V$ on the red channel. In the case of a chosen color depth of 24-bit, each color intensity can be adjusted within an 8-bit range which leads to a LSB corresponding to a $2.7\,mV$ output voltage. Within that constraint, one can program arbitrary patterns or pulses by programming an appropriate sequence of color intensities on each channel (*cf.* Section 6.1.2). The major advantages of a graphics board over an analog waveform generator are its low price and its ability to quickly simulate different consecutive trigger tower pulses. At a resolution of 2048×1536 pixels and a refresh rate of $60\,Hz$, each pixel is addressed for approximately $5\,ns$. The resulting pixel rate of $5\,ns/pixel$ is well suited for the intended emulation, since the rise time[3] of a real trigger tower signal is about $50\,ns$ and the actual pulse duration is about $700\,ns$ [47]. With the above settings, nine pixels are used to simulate the rising edge of a trigger tower signal. About 16 pulses can therefore be placed into a single line of the video output for each color.
The analog output of the graphics card is sent through a standard monitor cable and received by two 15 pin SUB-D connectors on the MCM Testboard.

5.2 The MCM Testboard

The MCM Testboard holds two components of the final PPM: an Analog Input Board and a MCM. A photograph of the MCM Testboard is shown in Figure 5.1; the block diagram in Figure 5.2 illustrates the boards major building blocks together with the most important data paths. A detailed description of the MCM Testboard is given in the following sections.

Power Supply and Control

The MCM Testboard is powered by applying $+8\,V$ and $-8\,V$ to the power connectors. Seven onboard power supplies provide the appropriate voltages for the MCM Testboard components. Four power supplies ($+5.0\,V$ digital, $+5.0\,V$ analog, -5.0 V analog, and $+3.3\,V$ digital) provide power to all components on the MCM Testboard except the MCM itself. The remaining three supplies provide power to the MCM: AVDD = $+5.0\,V$ analog, DVCC = $+3.3\,V$ digital, and AVCC = $+3.3\,V$ analog. They are completely independent from the other four supply voltages. This makes the MCM testing simpler as all voltages and currents in these three circuits are constantly monitored. Unusual voltage or current measurements would indicate a faulty device within that power circuit (*cf.* Table 5.1).

[3]The rise time of a signal denotes the time from its beginning to its maximum amplitude.

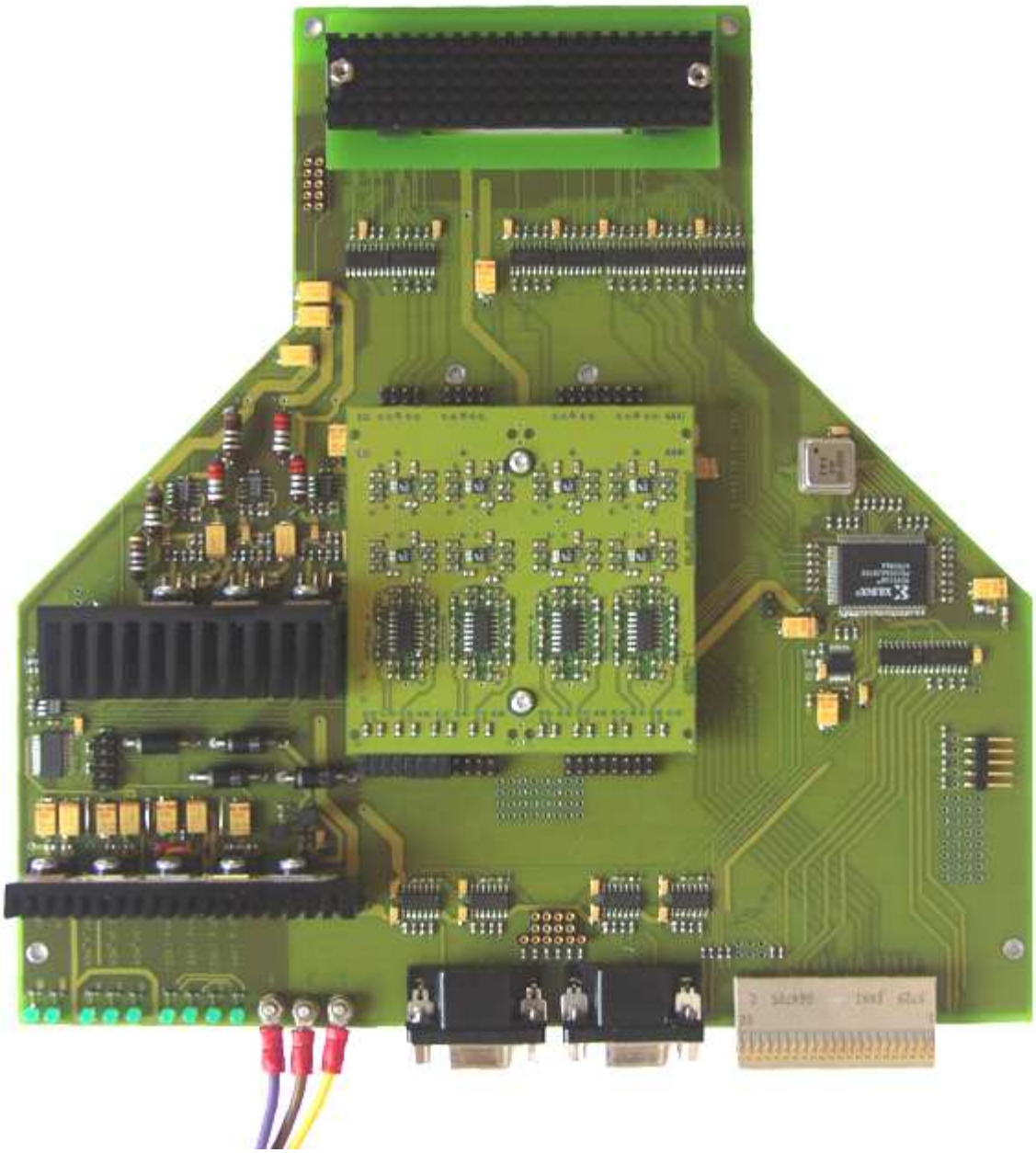

Figure 5.1: Photograph of the MCM Testboard.

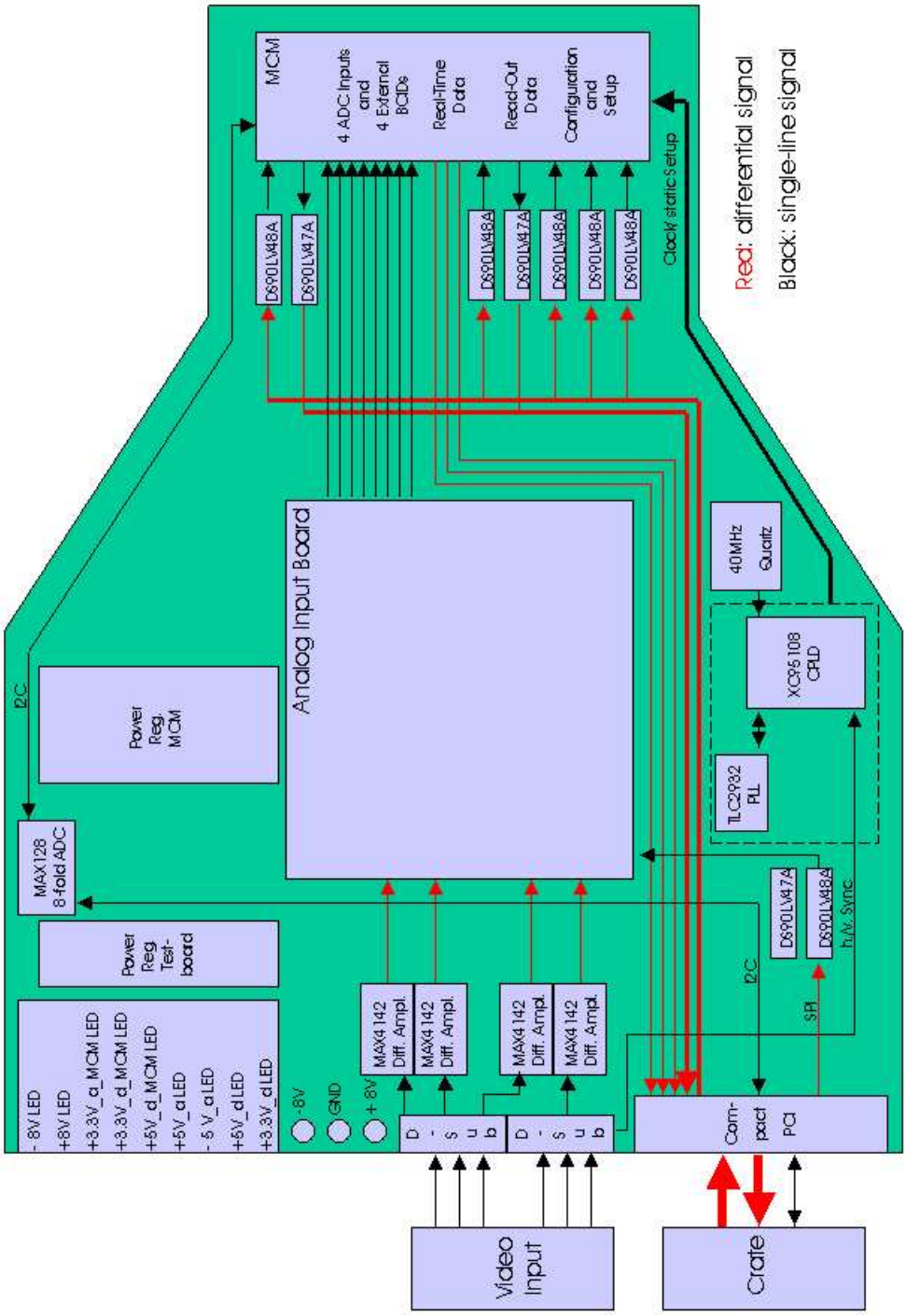

Figure 5.2: Block diagram of the MCM Testboard.

MCM Components	ADCs (AD9042)	LVDS Serializers (DS92LV1021)	PPrASIC	Phos4
AVDD $= +5.0\,V$ (analog)	✓			
AVCC $= +3.3\,V$ (analog)		✓		
DVCC $= +3.3\,V$ (digital)	✓	✓	✓	✓

Table 5.1: Power Supplies for all chips on the MCM [37].

Each current causes a small voltage drop across a sensing resistor which is amplified by an operational amplifier and then digitized by an eightfold ADC (MAX128 [48]). Besides monitoring the three MCM currents and voltages, the MAX128 reads out the temperature of the PPrASIC which can be measured by monitoring the current through a diode placed on the PPrASIC. All measurements can be read out via the I^2C-bus[4] that is explained in Section 6.2. All voltage supplies can also be checked optically: nine lit LEDs[5] on the MCM Testboard indicate their proper function.

Timing Control

All chips on the MCM are clocked with a frequency of $40\,MHz$. A Phase Locked Loop (PLL) is used to synchronize the $40\,MHz$ clock with the analog test signals generated by the graphics card. More precisely, the horizontal scan signal will be used for this purpose. The functionality of a PLL is illustrated in Figure 5.3.

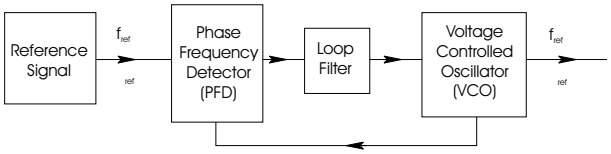

Figure 5.3: Scheme of a Phased Locked Loop (PLL).

A PLL is an electronic circuit with feedback coupling. The feedback coupling is used to match the frequency as well as the phase of the input signal of a Voltage Controlled Oscillator (VCO) to the frequency and phase of the VCO output signal. To achieve this, a Phase Frequency Detector (PFD) compares the VCO output with the reference signal. The PFD then produces an output pulse proportional to the phase difference between the two signals. This pulse is then smoothed by a Loop Filter and the DC[6] component of the smoothed pulse is fed back to the VCO input. This cycle is repeated until the frequency and phase difference between the reference signal and the VCO output is minimized. Once

[4] Inter-Integrated Circuit.
[5] Light Emitting Diodes.
[6] Direct Current.

this state is reached, it is maintained. Since the horizontal scan signal frequency is of the order of magnitude kHz, it has to be multiplied by a factor $N \approx 1000$ in order to simulate the $40\,MHz$ LHC clock. Therefore, a frequency scaler has to be inserted between the VCO and the PFD as shown in Figure 5.4.

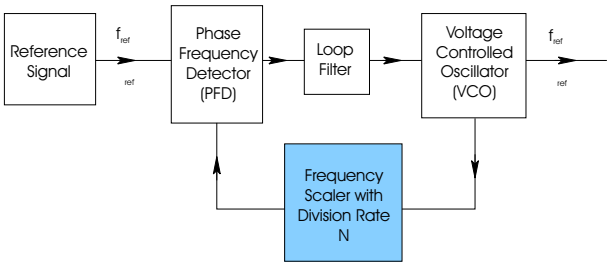

Figure 5.4: Scheme of a PLL with frequency scaler.

On the MCM Testboard, this circuit is realized by the Texas Instruments TLC2932 [49] which provides the VCO and the PFD. The Loop Filter is realized by external resistors and capacitors. The frequency scaler will be implemented in the Xilinx CPLD[7] XC95108 [50] as 10-bit counter with programmable final value. Because of the relation $f_{VCO} = f_{ref} \cdot N$, the programmable final value guarantees that the fixed $f_{VCO} = 40\,MHz$ output signal frequency can always be created, even if varying reference signal frequencies are used.
Furthermore, the CPLD is used to transform the highly asymmetric duty cycle[8] of the horizontal scan signal into a symmetric one, since the TLC2932 requires a symmetric input signal.
An additional $40\,MHz$ quartz was placed on the MCM Testboard to provide the MCM with a clock even if no input signal is applied to the MCM Testboard. This is done to avoid that the Phos4 makes a transition into an undefined state if no external clock is applied.

Differential Line Amplifiers

Four Maxim MAX4142 differential line receivers [51] receive the four analog video signals. The single line inputs are then converted into differential signals and amplified such that the input voltage range of $0 - 0.7\,V$ is mapped onto $0 - 2.5\,V$. Since the internal amplification of the MAX4142 is only $2\,V/V$, external resistors have to be used to raise the amplification factor to the desired value of 3.5. The output of the MAX4142 now complies with the input specifications of the subsequent Analog Input Board.

LVDS Drivers and Receivers

All data exchanged between the MCM Testboard and the PCBs in the VME crate have to be transmitted differentially to minimize noise. The I^2C-bus is an exception, since its

[7] Complex Programmable Logic Device.
[8] A duty cycle is the ratio of a signals HIGH period to its LOW period. It is said to be symmetric, if the HIGH period lasts exactly as long as the LOW period.

protocol does not allow a differential transmission [52]. All incoming differential signals are transformed into single line signals by one out of six 4-fold LVDS receivers (DS90LV048A [53]) by National Semiconductor. Two LVDS driver chips (DS90LV047A [54]) are used to transmit all differential signals to the crate system.

5.3 The VME Crate System

A set of three PCBs is used to receive the data arriving from the MCM Testboard. The general purpose motherboard functions as a Common Mezzanine Card (CMC) carrier for the Virtex CMC an the LVDS Receiver and Transmitter CMC (LVDS_r_t CMC). A schematic overview of the PCB set is shown in Figure 5.8. One FPGA on each board forms the centerpiece of the respective PCB. All PCBs will be described in detail after a brief introduction to FPGAs.

5.3.1 Field Programmable Gate Arrays

FPGAs are programmable devices with an internal array of logic blocks, surrounded by a ring of programmable input/output blocks, connected via dynamical connections. They are, like ASICs, designed to perform numerous parallel operations within one clock cycle. The primary advantage of FPGAs over ASICs is the programmability of the former chip type: a single FPGA can accomplish multiple tasks that can change with time, whereas the main functionality of an ASIC cannot be changed once the chip is produced. The major building blocks of FPGAs are:

- Blocks which perform various logic operations, *e.g.* the linking of two signals through a logical "AND", "OR", "XOR", etc. In the case of Xilinx FPGAs, these blocks are called Configurable Logic Blocks (CLBs).
- Input and output blocks (IOBs) form the interface between the CLBs and the external connections (pins) to electronic components outside of the FPGA. Some FPGAs, *e.g.* the Virtex-E series by Xilinx, provide several different signal output formats such as LVDS. Each pin can be used as an input, output or bidirectional access to or from the FPGA. Additionally, it can be made a high impedance pin.
- The routing network connects the above components dynamically and processes global signals like the clock and reset signals.

These components are distributed in a regular pattern throughout the FPGA. Programming a FPGA means to link the above parts in such a way that the intended task can be completed by using the wired logic blocks. Once a program is loaded - usually after a power-up sequence - the FPGA remains in the loaded state until a reset signal is sent or the power supply is cut.
Designing a FPGA code involves several steps. First, a source code is written in a Hardware Description Language (HDL). Most programmers use either Verilog[9] or VHDL[10] which

[9] Verifying Logic.
[10] Very high speed integrated circuit Hardware Description Language.

resemble in a certain way the C programming language. The code is then "synthesized" which means that the program is compiled into a netlist. The netlist corresponds to the HDL design using logical combinations of *e.g.* "AND" and "OR". Finally, the design passes a Place-And-Route (PAR) tool: during this step, the intended functionality of the design is mapped onto specific CLBs of a particular FPGA type. It is possible to specify a large variety of parameters such as the output format of the chip or the pins of certain or all input and output signals. This is done by inserting a so-called constraint file into the PAR process. The PAR output is then compiled into a bit stream which can be loaded into the real FPGA.
The current software packages used in the FPGA code design are the FPGA Compiler II developed by Synopsys [55] for the code synthesis and the Xilinx ISE 4.1 tool set [56] for the PAR process.

The General Purpose Motherboard

The general purpose motherboard is a 6U ($23.3\,cm$) high VME board. A photograph of the board is shown in Figure 5.5. Two CMCs can be plugged onto it.

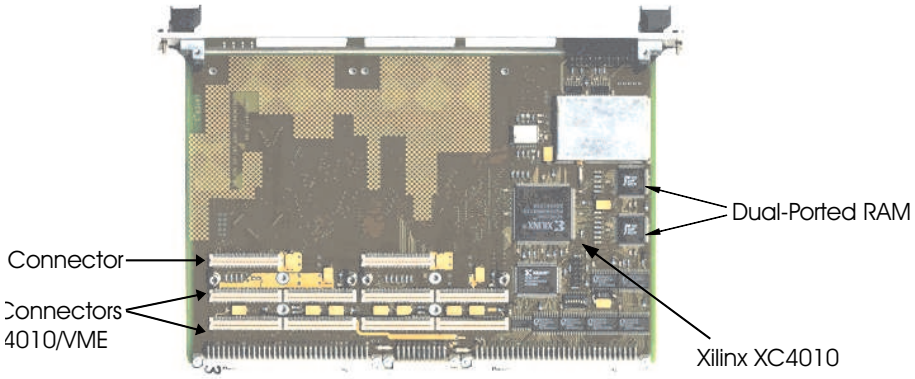

Figure 5.5: Photograph of the general purpose motherboard.

The centerpiece of the general purpose motherboard is a Xilinx XC4010XL FPGA [57]. It is connected to the VMEbus through a 32 KByte Dual-Ported RAM (DPRAM) module. Most of the FPGAs pins are connected to the SMD[11] connectors, thus providing access to the CMC daughterboards. A quartz on the motherboard generates the clock signal in a frequency range from $0.4 - 120\,MHz$ and distributes it to the XC4010 as well as to the daughterboard FPGAs. The motherboard FPGA is used as a controlling and configuration unit for the daughterboard FPGAs.

The LVDS Receiver and Transmitter CMC

One of the CMCs plugged onto the general purpose motherboard is the LVDS Receiver and Transmitter CMC (LVDS_r_t CMC). The LVDS_r_t board can be programmed to

[11] Surface Mounting Device.

serve as a LVDS sender board using the four LVDS serializer chips (DS92LV1021 [39]). Alternatively, the CMC can be configured as a LVDS receiver board by making use of the four LVDS deserializers (DS92LV1024 [58]). The actual configuration is implemented in the CPLD located on the front side of the board. In the test system described in this chapter, the CMC is programmed to act as receiving unit. Therefore, the LVDS_r_t CMC will be referred to as LVDS_r CMC in the following sections. The main component of the CMC is a Xilinx Virtex-E 50 FPGA (XCV50E) [42]. Figure 5.6 shows a picture of both board sides.

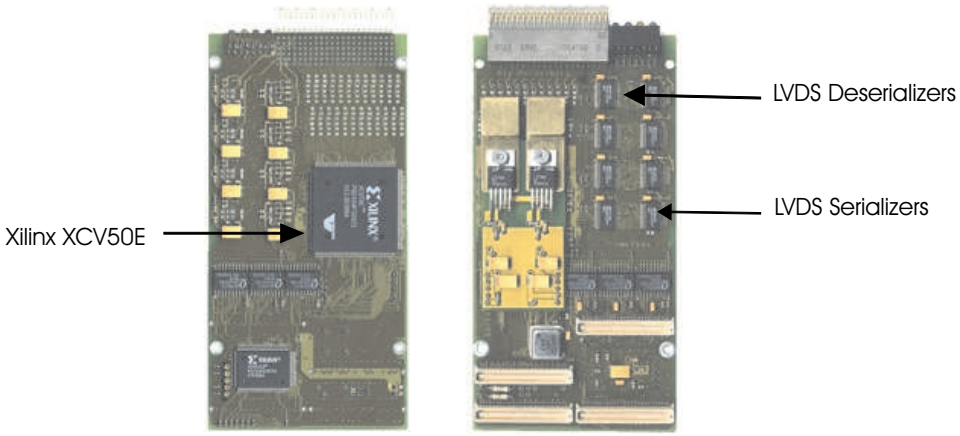

Figure 5.6: Photograph of the LVDS Receiver CMC.

The XCV50E is the only FPGA in the PCB test system capable of handling differential signals. This is why the XCV50E has to serve as the interface between the crate system and the MCM Testboard: the LVDS_r CMC receives all data arriving from the MCM Testboard. The three real-time channels are received by three LVDS deserializers and sent on to the S-Link connector indicated in Figure 5.5. All other signals (*e.g.* the ReadOUT data) are received by the XCV50E, since the signals have to be transmitted differentially via twisted pair cables. Configuration data such as the SPI data to the Analog Input Board or the PPrASIC configuration data must also be transmitted differentially.

The Virtex CMC

The second CMC is named Virtex CMC, since a Xilinx Virtex 300 (XCV300) FPGA [59] forms its centerpiece. A Static RAM (SRAM), $256K \times 36$ bit in size, is only accessible through the XCV300. The memory block is used as a buffer for all incoming data from the MCM Testboard. A photograph of the Virtex CMC is shown in Figure 5.7.

5.3.2 The Data Acquisition Process

A schematic overview of the test system and the dataflow through it is shown in Figure 5.8. The real-time data path is indicated in red, whereas the ReadOUT data path is illustrated in yellow. Configuration and setup data paths are shown in black. Figure 5.9 shows a photograph of the actual test system.

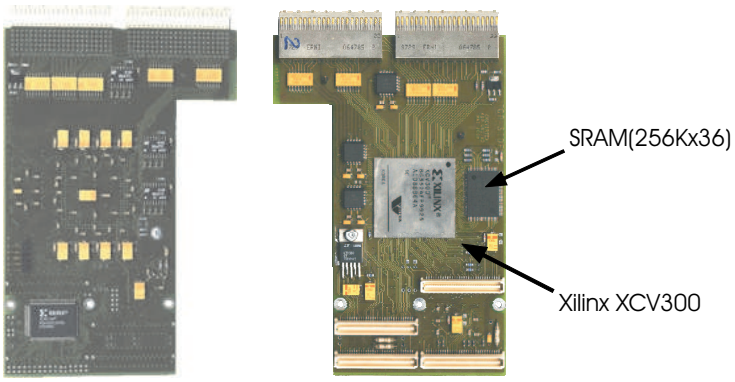

Figure 5.7: Photograph of the Virtex CMC.

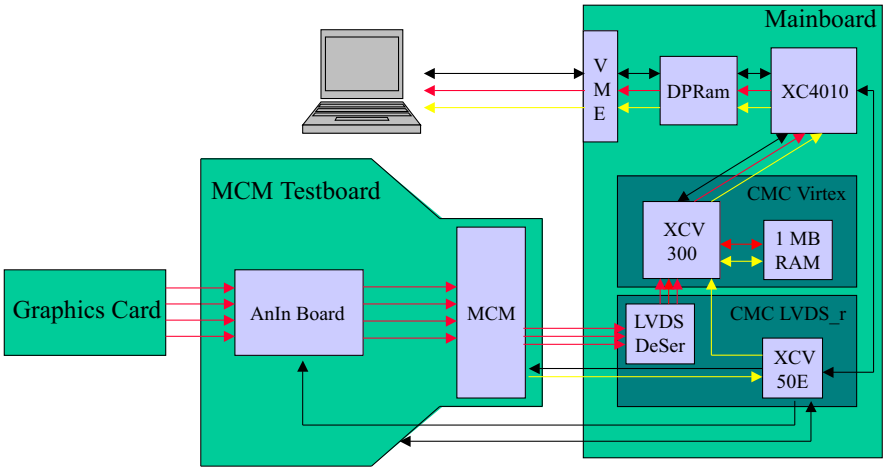

Figure 5.8: Block diagram of the MCM test system. The real-time data path is indicated in red, whereas the ReadOUT data path is illustrated in yellow. Configuration and setup data paths are shown in black.

In any case, a command is issued via the VMEbus to the DPRAM. It is then interpreted by the XC4010 and sent on to the appropriate daughterboard FPGA.

If one wants to read out real-time data, a command is issued to the XCV300. The daughterboard FPGA then starts to write data from the S-Link connectors, where the real-time data are sent to by the LVDS deserializers, into the SRAM. The acquisition process is stopped before the SRAM is completely filled. The data are then read back to the XCV300 and sent to the XC4010 via the SMD connectors. In order to permanently store the data, they have to be made available on the VMEbus. Therefore, the XC4010 stores them into the DPRAM from where they can be read out. The readout can now be compared to a set of data obtained from simulations or from a MCM that is known to function properly. A perfect match of both data sets is not mandatory for a MCM to pass the test: if an analog signal is digitized and later turned into an analog signal again, it will not be exactly identical to the input signal. The reason for this is that all electronic

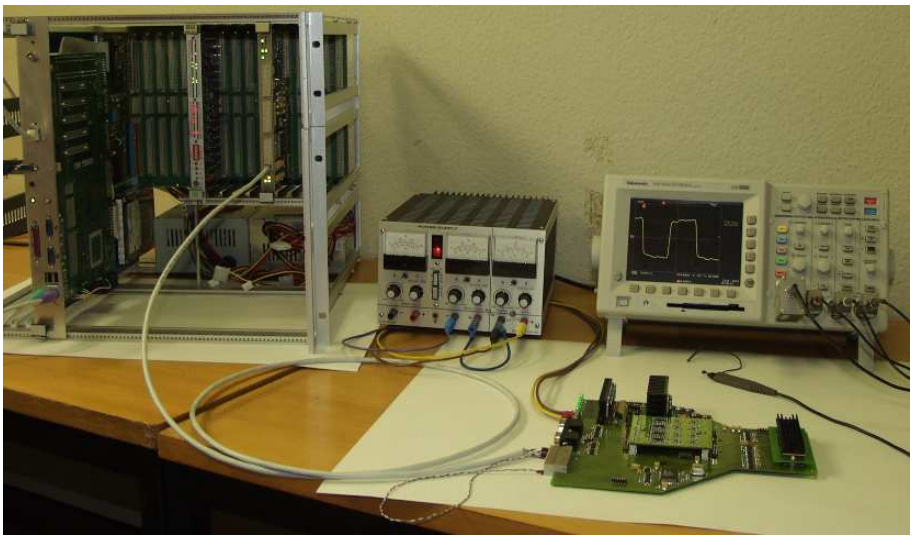

Figure 5.9: Photograph of the MCM test system.

components are non-ideal, *e.g.* the sampling time of ADCs is not constant but fluctuates slightly around the ideal sampling time (jitter).
In the case of collecting PPrASIC ReadOUT data, the data flow is similar to the one mentioned above. The only difference is that the data are first received by the XCV50E on the LVDS_r CMC.
A continuous readout of data is not possible since the VMEbus is far too slow to read out data with a rate of $40\,MHz$. It is also not possible to readout real-time data and ReadOUT data in parallel, since both data sets have to be buffered in the SRAM on the Virtex CMC. However, the test setup introduced in this chapter meets the requirements for a portable MCM test system that will be used at the MCM manufacturing company.

Chapter 6

Software and Firmware for the Pre-Processor Test System

This chapter describes the software and firmware developed for the hardware components introduced in the Chapter 5. After summarizing the software for the graphics card, emphasis will be placed on the FPGA firmware needed in order to receive and store incoming test data and to configure the MCM and MCM Testboard components.

6.1 Analog Inputs to the Test System

6.1.1 Test Beam Pulses

During fall 2001, a series of ATLAS test beam runs were conducted at CERN. Final modules of the HEC [47], hadronic tile [47], and EMB[1] [60] calorimeters described in Section 2.2.2 were installed and tested. In total, more than 400 analog calorimeter signals generated either by electrons and pions from test beams or by a calibration system were recorded with an oscilloscope (Tektronix TDS3034 [61]). These are the first analog pulses available from the mentioned detectors. Pulses from the HEC and hadronic tile calorimeters are exemplarily studied in the following sections.

HEC Calorimeter Test Beam Measurements

The test beam setup involved two final HEC modules. The geometrical extent of the modules covered the region between $1.5 < \eta < 3.2$ for the polar angle and $0 < \phi < 0.6$ for the azimuthal angle. Electrons with energies of 60, 120, and 148 GeV, as well as pions of 120 GeV were injected into the production modules.
A picture of the averaged signal of 120 GeV electrons is shown on the left side of Figure 6.1, whereas the right side shows the same plot on a different time scale and an additional single pulse in red. The pulse undershoot is characteristic to liquid argon calorimeter signal shapers.

[1] ElectroMagnetic Barrel.

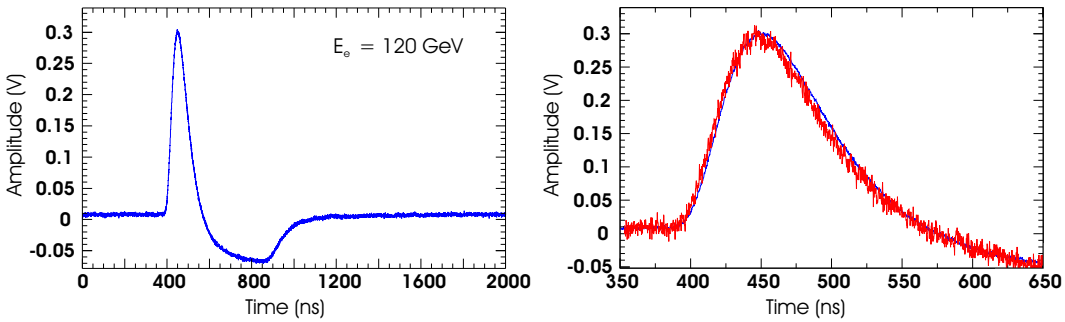

Figure 6.1: HEC calorimeter trigger tower test beam pulses. Left: Averaged signal of 120 GeV electrons. Right: same as left plus a single signal (red).

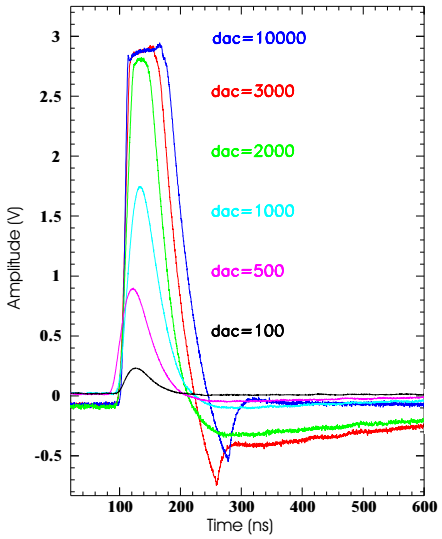

Figure 6.2: HEC calorimeter trigger tower calibration system pulses representing particle energies over the full dynamic range.

Figure 6.2 shows the trigger tower pulse shape for various calibration pulses. The given DAC values are arbitrary units. Starting at a pulse amplitude of about 2.8 V, saturation effects such as a distortion of the undershoot and the formation of a plateau were observed.

Hadronic Tile Calorimeter Test Beam Measurements

Electrons, muons and pions of 180 GeV were injected into two extended hadronic tile calorimeter modules that covered the region of $0.8 < \eta < 1.6$ and $0 < \phi < 0.1$ [47]. Figure 6.3 shows an averaged trigger tower pulse caused by 180 GeV pions on the left hand side, and the same pulse on another time scale along with a single pulse on the right hand side. The bulge visible in the left plot is a result of a transmission cable reflection. Figure 6.4 shows the trigger tower pulse for various injected electric charges: saturation-induced distortions are visible above a signal amplitude of about 3 V corresponding to an injected charge of 160 pC.

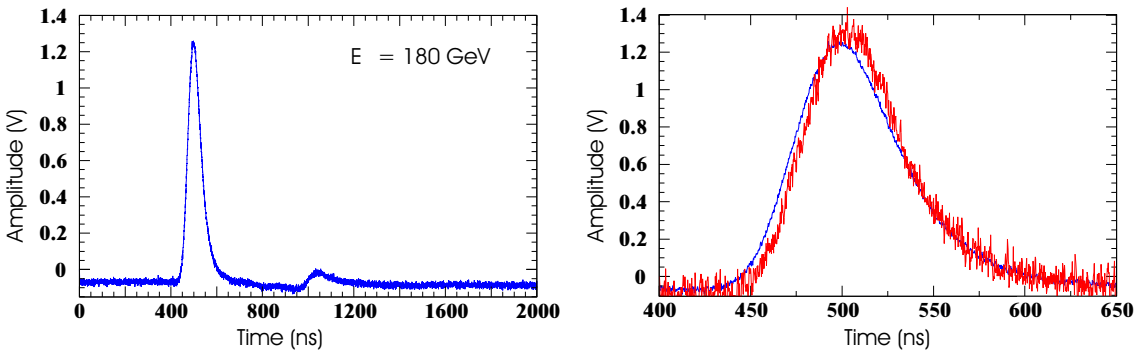

Figure 6.3: Hadronic tile calorimeter test beam pulses. Left: Averaged signal of 180 GeV pions. Right: same as left plus a single signal (red).

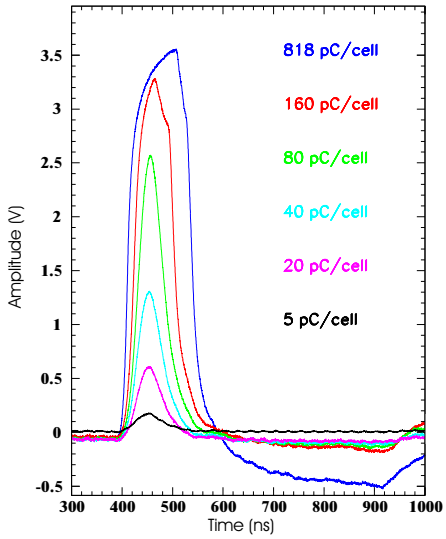

Figure 6.4: Hadronic tile calorimeter trigger tower pulses resulting from various injected calibration charges.

6.1.2 Simulating Pulses with a Graphics Card

A graphics card is used to simulate the trigger tower signals obtained in the previously described test beam runs. The C++ Graphical User Interface (GUI) toolkit Qt developed by Trolltech [62] is used to program a commercial graphics card that acts as the input signal generator for the MCM test system. Depending on a keystroke, the program displays various pulses on either one of the two graphics card output connectors.

Every test beam pulse was stored in a separate ASCII file each of which consists of 10,000 voltage measurements. Given the total signal length of 2 μs per recorded event, this corresponds to a time resolution of 200 ps per voltage value. 25 voltage measurements are merged into a single value in order for each result to correspond to a measurement extending over 5 ns. This is achieved by computing the arithmetic average of every 25 measurements and storing the resulting 400 values in a new file. This procedure results in

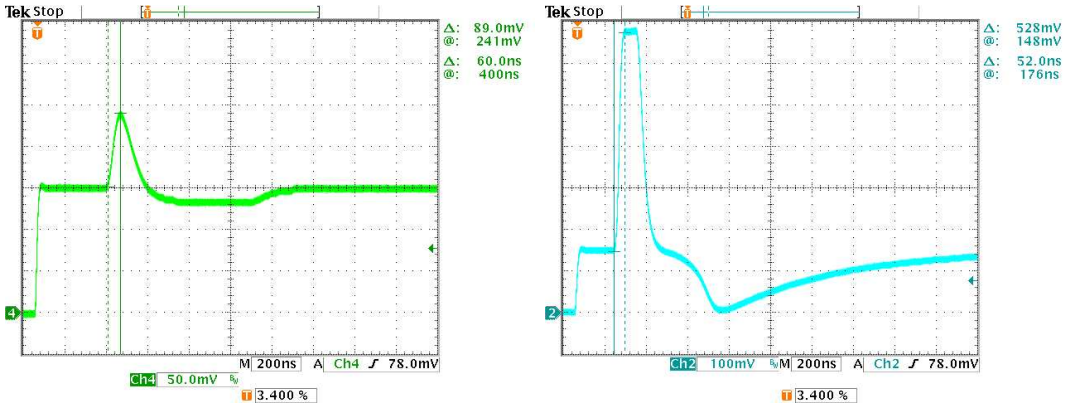

Figure 6.5: Simulation of HEC calorimeter test beam and calibration pulses. The unit length in x direction corresponds to 200 ns, whereas the unit length in y direction corresponds to 50 mV in the left picture and 100 mV in the right picture. The zero line is indicated by the numbers 4 and 2, respectively, on the left side of each picture. Left: Test beam pulse caused by a 120 GeV electron. Right: Saturated pulse.

a suppression of high-frequency noise. Each averaged value is represented by a pixel of a certain color. The intended pixel rate of 5 $ns/pixel$ (*cf.* Section 5.1) assures the temporal consistency of the test beam measurements with the emulation. In total, about 240 test beam files were converted into a suitable format in that way.
The next step consists of mapping the averaged data onto values between 0 and 255 since each color intensity is adjustable within an 8-bit range if the overall color depth is set to 24-bit (red, green, and blue). Due to either the liquid argon calorimeter signal shapers or saturation effects, negative voltages are comprehended in the data sets. Therefore, a base line shift has to be implemented in the C++ program, since the graphics card can only output positive voltages between 0 and 0.7 V. The maximum color intensity is assigned to 3.8 V, for this is the maximal voltage recorded in the test beam data sets. Correspondingly, the measured voltage minimum ($-0.8\,V$) is mapped to 0 V output on the graphics card.
The actual graphics card output can be monitored by attaching oscilloscope probes to a standard monitor cable that is plugged into one of the two graphics card output connectors. For this purpose, the same oscilloscope is used as for the test beam measurements. Figure 6.5 shows a simulated 120 GeV electron pulse from the HEC calorimeter on the left hand side, whereas a saturated HEC pulse is illustrated on the right hand side. Both pictures show signal shapes comparable to the original pulses shown in Figures 6.1 and 6.2. The signal rise time is indicated by a Δ in the upper right corner of each picture.
In addition to simulating test beam pulses, an ideal pulse shape was implemented in the code as an analytical function [63] describing the pulse shape of a liquid argon calorimeter. It is shown in Figure 6.6 along with the pulses from Figure 6.5. This demonstrates the possibility of simultaneously sending different pulses on each color output without affecting the other two outputs.

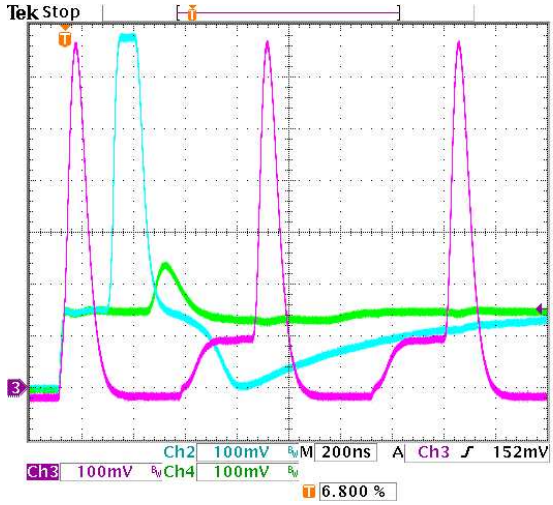

Figure 6.6: Simultaneous signal generation on all three color outputs. The unit length in x direction corresponds to 200 ns, whereas the unit length in y direction corresponds to 100 mV. The zero line is indicated by the number 3 on the left side of the picture.

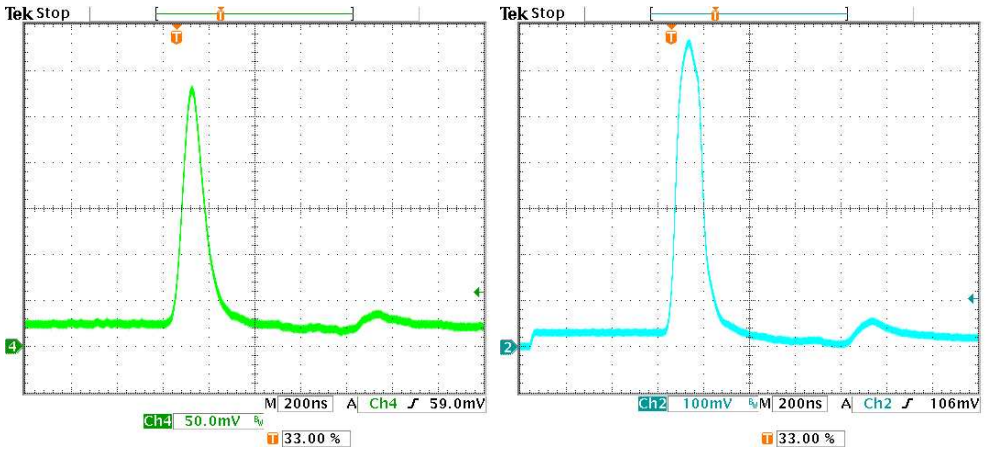

Figure 6.7: Simulation of hadronic tile calorimeter test beam and calibration pulses. The unit length in x direction corresponds to 200 ns, whereas the unit length in y direction corresponds to 50 mV in the left and 100 mV in the right picture. The zero line is indicated by the numbers 4 and 2, respectively, on the left side of each picture. Left: Test beam pulse caused by a 180 GeV pion. Right: Saturated pulse caused by the injection of 160 pC.

Figure 6.7 shows pulses that simulate tile calorimeter signals. The simulation of a $180\,GeV$ pion pulse is shown on the left, a simulation of the saturated pulse caused by the injection of $160\,pC$ on the right (*cf.* Figures 6.3 and 6.4).

Besides reproducing test beam pulses, the graphics card output was analyzed in terms of linearity of the output voltages, noise, and crosstalk. The output voltage of the three color outputs differed within 2% over the entire voltage range. The noise level lies at about $20\,mV$. This is due to the inaccuracy of the video output, the unshielded probe adapter, and the oscilloscope probes themselves. However, a low-pass filter mounted on the MCM Testboard and the MCM itself will effectively suppress most of the noise. In the case of the above pictures, the low-pass filter is realized by the internal low-pass option of the oscilloscope that cuts off all signals with frequencies above $20\,MHz$.

Minor shape discrepancies between the real pulses and the simulated graphics card signals are due to the averaging of the original test beam data. However, the overall resemblance in terms of signal length, rise time, and shape is convincing and proves the usability of the program as a realistic signal generator for the MCM test system.

6.2 FPGA Firmware

As stated in Section 5.3, three FPGAs are responsible for collecting test data and configuring the MCM Testboard and the PPrASIC. The FPGAs are provided with a $40\,MHz$ clock signal generated by a quartz on the general purpose motherboard. An 8-bit wide bus processes commands issued by the master (XC4010) to the daughterboard FPGAs. A 32-bit wide bus transfers data words between the XC4010 and the XCV50E or XCV300. All communication between the FPGAs is a so-called dual-handshaked communication process controlled by two flag bits: the STROBE flag bit is pulled down by the master FPGA to indicate that a new command is available on the command bus. The slave then reacts by asserting a response flag bit, the BUSY signal. After completion of the task, the slave FPGA releases the BUSY line and causes the master to release the STROBE line as well. This procedure is illustrated in Figure 6.8.

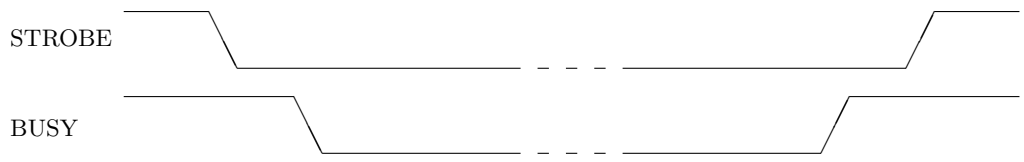

Figure 6.8: A dual-handshaked communication.

6.2.1 The XCV50E

The XCV50E is the only FPGA in the test system that is capable of handling differential signals. Therefore, it has to accomplish all communication between the set of PCBs and the MCM Testboard. Besides the differential output, the XCV50E also serves as the I^2C-Master FPGA.

The I^2C Interface

The I^2C protocol is a serial data protocol developed by Philips [52]. It is well suited for controlling purposes: in the case of the MCM test system, the I^2C-bus is used to configure the Phos4 on the MCM and to read out the MAX128 voltage and current control data (*cf.* Section 5.2). The I^2C protocol allows the communication between a large number of devices, including several master devices, via two signal lines. In this context, a master device is *e.g.* a FPGA, an ASIC, or a microprocessor that is actively requesting data from another device on the bus. Devices which are only passively reacting to one of these requests are referred to as slaves. The only I^2C master in the MCM test system is the XCV50E, whereas the MAX128 and the Phos4 are slave devices. The bus speed is set to 100 kBit/s for this test environment.
The two I^2C-bus lines are both bidirectional wires connected to pull-up resistors[2]. One line serves as Serial Clock (SCL) line, the other as Serial Data (SDA) line. The beginning of a transmission is always initiated by a START signal generated by the master. It is defined as a HIGH to LOW transition of the SDA line while SCL is HIGH. A STOP signal is defined as a LOW to HIGH transition of SDA line while SCL is HIGH and is issued by the master (*cf.* Figure 6.9) at the end of a transfer cycle.

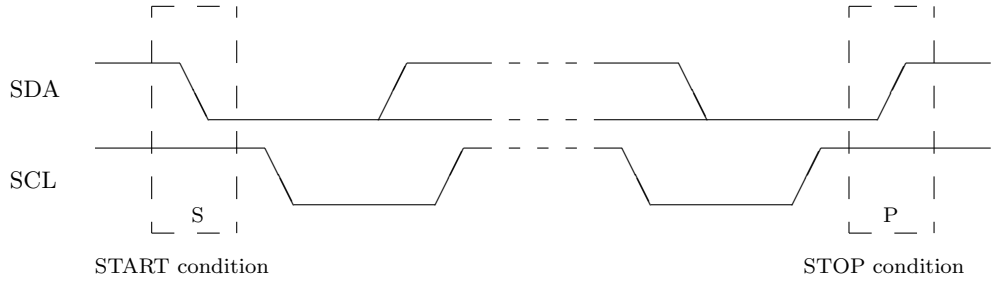

Figure 6.9: START and STOP conditions of the I^2C protocol.

After initiating a data transfer, the master pulls down the SCL line. A slave device can hold down the SCL line as long as it needs to complete a task or react to a command. Therefore, the SCL line can remain LOW, even if the I^2C master releases the line. In this case, the master waits for the slave to release the line before sending an 8-bit data word onto the bus. During the HIGH period of the serial clock, all data have to remain stable. Data changes are only allowed while SCL is low (*cf.* Figure 6.10).

[2]Pull-up and pull-down resistors assure that given no other input, a circuit assumes a default value. In the case of a pull-up resistor, this default setting is HIGH.

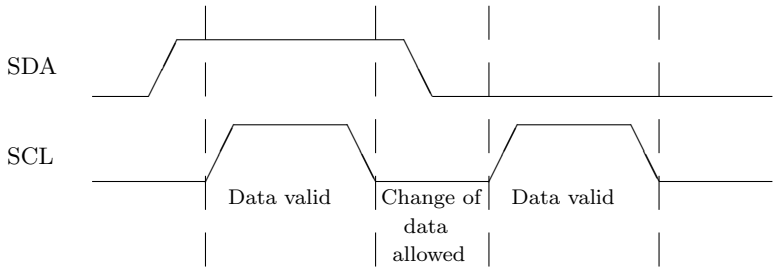

Figure 6.10: Bitwise data transfer on the I^2C-bus.

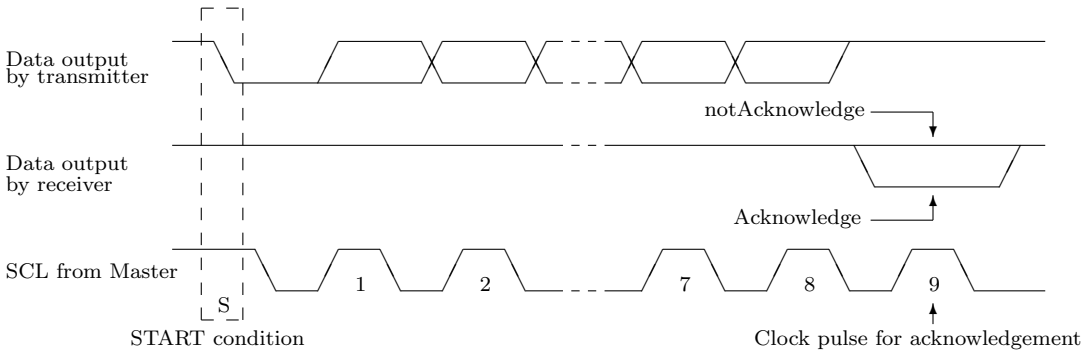

Figure 6.11: Acknowledge on the I^2C-bus.

After the transmission of the 8-bit data word, the master generates a ninth SCL cycle. However, the SDA line is driven by the slave during that period: it is pulled LOW if the data have been received successfully, and set HIGH otherwise (*cf.* Figure 6.11).
The first data word submitted by the master consists of a 7-bit I^2C address and a bit which determines the direction of the following data transfer. If a slave is addressed properly, it reacts by pulling SDA LOW during the ninth clock cycle. The next 8-bit word is either sent or received by the master followed again by an acknowledge bit from the slave or master device, respectively. An arbitrary number of these 9-bit data words can now be transmitted before a STOP signal concludes the data transfer.
An existing I^2C source code provided by OpenCores [64] was chosen to be implemented in the XCV50E since it provides all functionality necessary to configure the Phos4 and to read out the MAX128.

The Serial Peripheral Interface

The SPI is a rather simple serial interface that uses three data lines: Data-In (DIN), clock (CLK), and Chip Select (CS). The only devices that are configurable through the SPI are the MAX529 DACs on the Analog Input Board (*cf.* Section 4.2.1). Additionally, each MAX529 has a Data-Out (DOUT) pin. These four chips are linked consecutively (daisy chain): the DOUT pin of the first MAX529 is connected to the DIN port of the

second MAX529, and so forth. A 16-bit shift register is implemented in each DAC. With every clock tick, the current DIN value is stored into the LSB of the shift register. The previously stored LSB is shifted to the second position pushing the previously second bit to the third position et cetera. The Most Significant Bit (MSB) of the first MAX529 is sent to the DIN pin of the second MAX529. Therefore, 64 bits are necessary to configure four DACs. The configuration becomes effective when the CS signal is sent.

The Serial Interfaces of the Pre-Processor ASIC

Each Pre-Processor ASIC features two serial interfaces (*cf.* Section 4.2.2). Four data lines are used to communicate with the PPrASIC: Clock, Frame, DataIn, and DataOut. The latter two allow a simultaneous reading and writing from and to the PPrASIC. The Frame signal which is sent every 13 clock cycles denotes the beginning of a 13-bit long data word. Data sent to the PPrASIC are either commands or configuration settings for the internal registers. The MSB of the 13-bit word decides which type of data is currently transferred. In the case of data sent by the PPrASIC one has to distinguish between ReadOUT and ReadBACK data. ReadBACK data are defined as contents of internal PPrASIC registers and memory cells. ReadOUT data are all data that are used to verify trigger decisions. Again, the MSB is used as a flag bit to denote which type of data is processed.
For a more detailed description of the PPrASIC serial interface refer to [36] and [65]. The first functional tests of the PPrASIC serial interfaces will make use of the FPGA source code developed for the RemFPGA [43].

6.2.2 The XCV300

The primary task of the XCV300 is to store incoming real-time, ReadBACK, and ReadOUT data into the SRAM also located on the Virtex CMC. A first series of tests were conducted that successfully wrote data from VMEbus into the SRAM, first passing the XC4010 and the XCV300. The data were then read back into the DPRAM and read out via VMEbus onto hard disk. Another design was written to feed trough the incoming real-time LVDS data onto LEDs located at the front panel of the Virtex CMC. This allows an optical comparison of the LVDS data received by the daughterboard with the data observed on an oscilloscope. This will be discussed in further detail in Chapter 7.

6.2.3 The XC4010

The XC4010 represents the master FPGA of the set of PCBs. Its main task is to act as the interface between the CMC daughterboards and the VMEbus. All commands are sent via VMEbus into the DPRAM [66] accessible by the XC4010. The DPRAM is 8K×32 bit in size and is equipped with two special interrupt registers located at the two highest addresses 1FFE and 1FFF (both HEX). If data are written on the latter address via VMEbus, a mailbox interrupt signal is generated and sent to the other port, namely the XC4010. Similarly, the XC4010 creates an interrupt signal on the VME side by writing data to the address 1FFE (HEX). However, the VMEbus driver currently used is not capable of handling interrupts. An overview of the DPRAM address space partitioning is given in Table 6.1.

DPRAM Address (HEX)	Use
1FFF	Command and Block Size
1FFE	Confirm Command
1FFD	Terminating Code
1FFC	Start Address
1FFB	Confirm Start Address
1000 - 1FFA	Configuration Data
0000 - 0FFF	Readout Data

Table 6.1: Address space partitioning for the DPRAM.

To facilitate the MCM testing, a command processor approach was chosen to be implemented in the XC4010: the FPGA consecutively works through a set of instructions or data previously stored into the DPRAM via VMEbus. A command interpreter has been implemented in the form of a twofold state machine. The hierarchically higher state machine is divided into the following states:

- IDLE. This state is persistently held as long as no mailbox interrupt signal is issued by the DPRAM.
- CHECKCOM. Succeeding a mailbox interrupt signal, this state interprets the 32-bit data word stored in the command address of the DPRAM using a second state machine.
- SENDDPRAM. This state sends a 32-bit word to the DPRAM where it can be read out via VMEbus.
- READDPRAM. A 32-bit data word is read from the DPRAM.
- WRITE300. This state is used to issue a 32-bit word on the data bus accessible to the XCV300 and XCV50E daughterboard FPGAs.
- READ300. A 32-bit data word sent by either the XCV300 or XCV50E is stored into an internal register.

Each command received by the XC4010 is confirmed by sending it back to the address 1FFE (HEX). The 32-bit command word itself consists of an 8-bit FPGA command (the eight MSBs) and a 12-bit block size argument (the twelve LSBs). All bits in between are left unused. However, it is possible to easily enhance the command state machine at a later stage if an 8-bit FPGA command word turned out to be insufficient.
If data are sent to the test system, the command decides which type of data is stored at the next DPRAM address, *e.g.* configuration data for the PPrASIC, I^2C commands, or data for the SPI. In this case, the block size indicates how many data words have been stored in the DPRAM, *i.e.* how many instructions have to be worked through in order to complete the writing cycle. Then, the data word stored at 1FFC (HEX) is read by the

XC4010. It denotes the starting address of the command. This could, for example, be the I^2C address to write to. The starting address is confirmed by sending it back to the 1FFB (HEX) address of the DPRAM. At that point, the appropriate daughterboard FPGA is addressed by the XC4010 and commences its operation. A terminating signal is issued by the XCV300 or XCV50E after completion of the task. Finally, the XC4010 sends a code to the DPRAM address 1FFD (HEX) to indicate that the test system is ready for new input.
In the case of a read cycle, the starting address is either the I^2C or the SRAM address to read from. The block size denotes the number of data words that are to be read out. All other steps are identical to the writing cycle.

6.2.4 Firmware Status

Extensive tests were conducted to test the interface between VMEbus and the PCB set. The XC4010 states responsible for all interactions with the DPRAM were successfully implemented and thoroughly tested. As far as the dual-handshaked communication between master and slave FPGAs is concerned, problems arose which are not solved at the time of writing. The possible explanations range from hardware problems caused by new hardware components, *e.g.* the LVDS_r CMC, to software issues of the FPGA Compiler II which is possibly responsible for difficulties that occurred during the development of the RemFPGA code [43].
Some tests have been carried out to test the I^2C interface. However, no I^2C component on the MCM Testboard has yet been addressed. Compilable source code was written for the serial interface for the PPrASIC and the SPI. However, neither one of them was tested in practice due to time constraints.

Chapter 7

Measurements and Results

The measurements presented in this chapter constitute the first tests of final Pre-Processor hardware components, namely an Analog Input Board and a fully assembled MCM. The tests included basic electrical tests as well as a first check of the real-time LVDS data generated by the MCM.

7.1 Power Tests of the Pre-Processor ASIC

A series of PPrASICs that consists of roughly 200 dies and another 400 chips on two wafers[1] was manufactured in a first production cycle. 14 individual PPrASICs were powered and provided with a clock signal using frequencies up to $50\,MHz$ [67]. The results of nine tested PPrASICs are shown in Figures 7.1 and 7.2 with each line corresponding to a single PPrASIC. The difference between the two plots is the RESET setting of the dies: in the first picture, the ASICs are not reset, whereas the RESET is applied constantly during the measurements of the second plot. In the former case, the number of toggling flip-flops[2] is higher than in the latter case resulting in a lower current consumption of the reset chips.

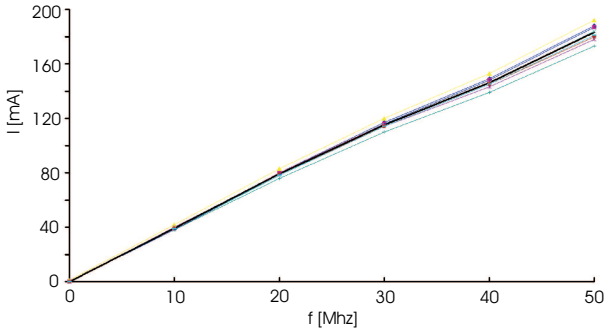

Figure 7.1: Current consumption of nine PPrASICs without RESET as a function of the clock frequency. Each line corresponds to a single chip. No analog input was applied.

[1] A wafer is a thin slice of polished silicon containing numerous chips side by side.
[2] Flip-flops are digital 1-bit storage devices.

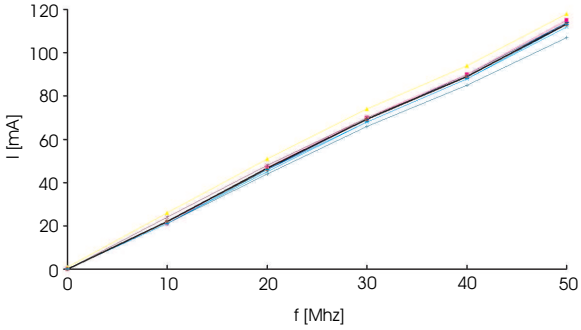

Figure 7.2: Current consumption of nine PPrASICs with applied RESET as a function of the clock frequency. Each line corresponds to a single chip. No analog input was applied.

The plots show a consistent linear relation between the current consumption and the applied clock frequency. All nine dies differ only slightly from each other in terms of current consumption. The maximal current consumption is reached for a clock frequency of $50\,MHz$: about $180\,mA$ without applied RESET and $110\,mA$ in the RESET mode. Four out of the five remaining dies were damaged before the power test and the last ASIC showed an augmented current consumption pointing to a short circuit within the chip. As a matter of fact, an infrared camera was capable to pinpoint the location of the short circuit to a memory cell of the PPrASIC.
A test setup for a large scale wafer test is currently being developed [68]. This is necessary, in order to allow a preselection of properly working PPrASICs directly on the wafers. Faulty dies can be tagged so that they are not tested or used any further. The wafer test involves a second MCM Testboard with a MCM that does not have a PPrASIC bonded onto it. Instead, the MCM will be connected to the PPrASICs on the wafers via an adapter board and a needle card specifically designed for this purpose.

7.2 Tests using the MCM Testboard

After first electric tests of the MCM Testboard, a fully assembled MCM was plugged onto the PCB. A signal generated onboard was used as input to the test system. The resulting real-time MCM output was monitored with an oscilloscope and optically with the help of LEDs on the LVDS_r CMC. These tests will be described in detail in the following sections.

7.2.1 Electric Tests of the MCM Testboard

The electric tests involved the isolated MCM Testboard without MCM but with an Analog Input Board plugged onto it. No analog input was applied to the Testboard. All configurable chips are in their default states. After ensuring that all voltages remained on a constant level, a fully assembled MCM was added to the test system. Three voltage drops across the three sensing resistors that monitor the MCM power supplies (*cf.* Section 5.2) were measured. The consequential results are summarized in Table 7.1.

MCM Power Supply	Sensing Resistors [Ω]	Voltage Drop [mV]	Current [mA]	Power [W]
AVDD = +5.0 V	0.44	204	464	2.32
AVCC = +3.3 V	1.5	10	7	0.02
DVCC = +3.3 V	0.32	109	341	1,13

Table 7.1: Results of electrical measurements on the MCM Testboard.

In total, the power consumption of the MCM is about 3.5 W which is below the estimated value of roughly 5.5 W [37]. The main reason for the difference is the PPrASIC which consumed only about 0.5 W in the first tests instead of 2.5 W as estimated. One expects the power consumption to increase considerably once the PPrASIC is processing data and the serial interfaces and memory cells are put into operation.

7.2.2 Functional Tests of the MCM

One of the power-tested PPrASICs was bonded on the MCM used for the first functional tests on the MCM Testboard. So far, these tests did not include the graphics card as pulse generator, nor the PCB set as receiving station. The former could not be used since the needed PLL has not been implemented in the CPLD firmware yet whereas the latter was not applicable because of the mentioned firmware problems of the Xilinx FPGAs (*cf.* Section 6.2.4). Furthermore, all chips are in their default states as no configuration data were loaded.
The first functional test consisted of requesting a LVDS synchronization pattern from the LVDS serializers on the MCM. The test result is shown in Figure 7.3.

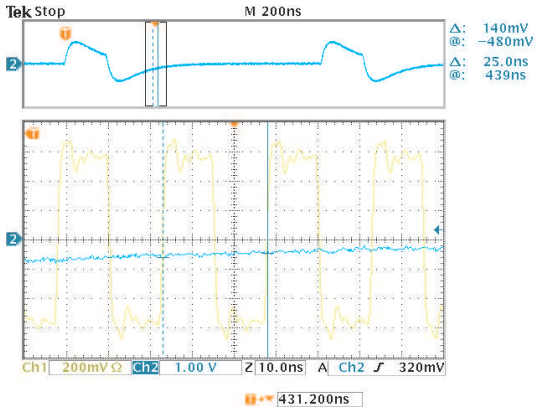

Figure 7.3: LVDS synchronization pattern (yellow) issued by the MCM LVDS serializers. A unit length in x direction corresponds to 10 ns, whereas the unit length in y direction corresponds to 200 mV for the LVDS data and 1 V for the input signal. The zero line is indicated by the number 2 on the left side of the picture.

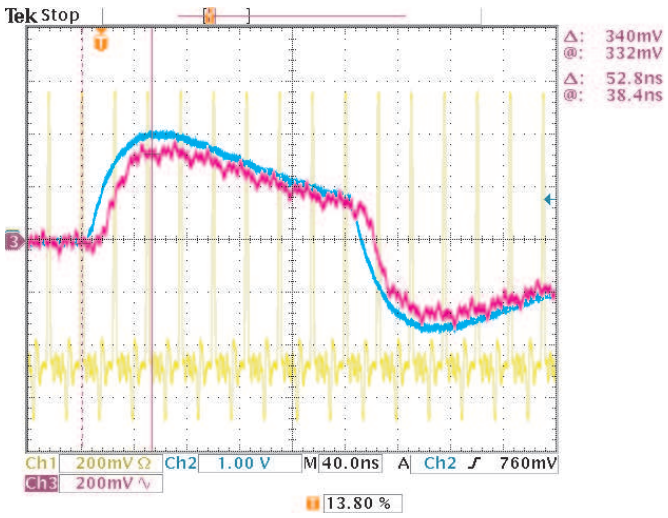

Figure 7.4: Study of the analog input signal. The blue graph shows the signal before reaching the Analog Input Board, the red curve corresponds to the signal after the Analog Input Board. The empty LVDS output of the MCM is shown in yellow. A unit length in x direction corresponds to $40\,ns$, whereas the unit length in y direction corresponds to $200\,mV$ for Channels 1 and 3 and $1\,V$ for the input signal. The zero line is indicated by the number 3 on the left side of the picture.

As stated in Chapter 4, a LVDS data transmission cycle comprises a START bit followed by ten data bits and a STOP bit. A synchronization pattern is a predefined sequence of data bits: the first five bits are set ("1"), the last five are zero. The blue pulse in Figure 7.3 is the analog input pulse which is of no meaning for this test, the yellow curve constitutes the synchronization pattern 11_1110_0000 constantly sent by the LVDS serializers.

A transmission of the synchronization pattern to the set of PCBs was successfully tested by connecting the MCM Testboard to the LVDS_r CMC via twisted pair cables. The LVDS deserializers on the LVDS_r CMC "locked" to the synchronization pattern which proves their proper functioning and the feasibility of the data transmission from the MCM Testboard to the set of PCBs in the crate.

As an alternative to the graphics card output, a signal generated from the $40\,MHz$ quartz clock pulses serves as input to the MCM. This is realized by modifying the Testboard CPLD firmware in such a way that a signal with a frequency of $2.5\,MHz$ is created. That signal is fed into the connectors preceding the Analog Input Board through a resonant circuit which consists of a coil of $4.7\mu H$ and a capacitor of $820\,pF$. The resulting analog input pulse is shown in Figure 7.4. The signal length and the rise time of about $50\,ns$ – indicated in the upper right corner of the picture – closely match the intended time parameters of real calorimeter trigger tower pulses and, therefore, should lead to an non-zero real-time data output of the PPrASIC. However, the response to the input signal is not visible in Figure 7.4 as the data processing through the MCM takes more clock

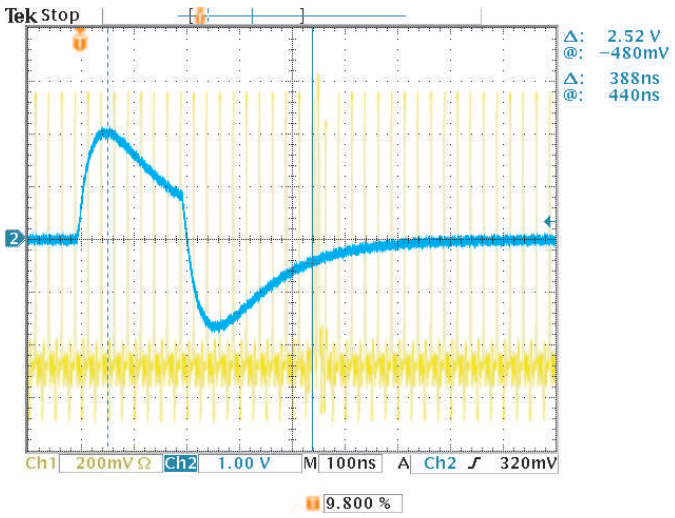

Figure 7.5: Analog input pulse and BCID output on the real-time Jet/Energy-Sum LVDS channel. A unit length in x direction corresponds to $100\,ns$, $200\,mV$ in y direction for the LVDS data and $1\,V$ for the analog input signal. The zero line is indicated by the number 2 on the left side of the picture.

cycles than shown. The red curve illustrates the AC[3] coupled input signal after passing the Analog Input Board. The pulse takes about $8\,ns$ to pass the MCM Testboard before reaching the MCM. The LVDS data (yellow) are zero in the shown time frame, except for the START bit, since the CPLD no longer requests a synchronization pattern.
Figure 7.5 shows the same input signal and the MCM LVDS output of the Jet/Energy-Sum channel on a longer time scale. After $388\,ns$, the LVDS output pattern changes to a non-zero value. This time interval – indicated by the two blue vertical lines – corresponds to about 16 LHC bunch-crossings which is exactly the specified number of bunch-crossings needed for the MCM to output a BCID result after recognizing a signal peak [26].
A close-up view of the LVDS output is shown in Figure 7.6. The blue vertical lines tag the START bit of the time slot in which the non-zero data are transmitted and the START bit of the following time frame. The LVDS data correspond to the bit sequence 01_0011_0000. An interpretation of the data will be given in Section 7.3.
Figure 7.7 shows a close-up view of the second, a Cluster Processor, real-time LVDS output channel that is also transmitting non-zero data. In this case, however, non-zero data is transmitted in two consecutive time frames. The second time frame corresponds exactly to the time frame of the non-zero Jet/Energy-Sum LVDS data (*cf.* Figure 7.6). The bit pattern for the first data set is 00_0100_1100 and 01_0000_0000 for the second. The blue vertical lines mark the first time frame.
The second Cluster Processor LVDS channel output is shown in Figure 7.8. All output in the respective time frames is constantly 00_0000_0000.

[3] Alternating Current.

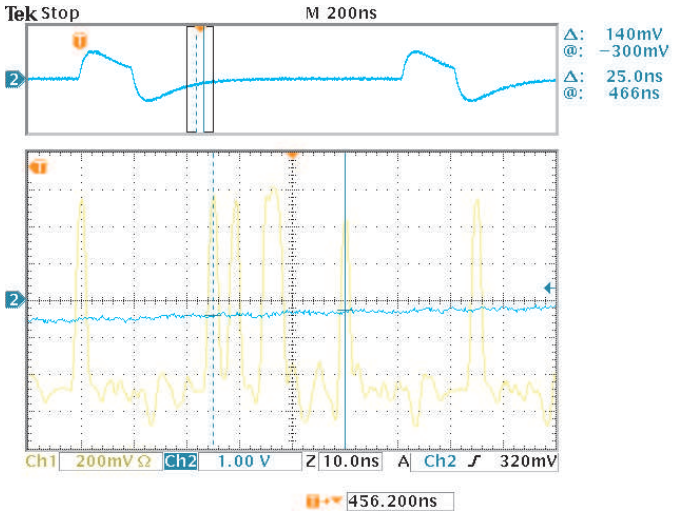

Figure 7.6: Close-up view of the BCID pattern generated by the PPrASIC as a consequence of the pulse shown in the upper part of the picture. These data are transmitted to the Jet/Energy-Sum Processor. The unit length in x direction corresponds to $10\,ns$, $200\,mV$ in y direction for the LVDS data, and $1\,V$ for the input signal. The zero line is indicated by the number 2 on the left side of the picture.

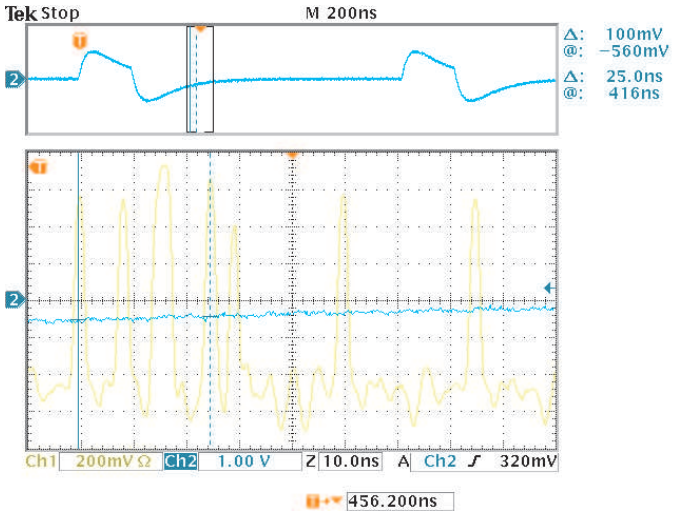

Figure 7.7: Close-up view of the LVDS output channel that sends non-zero data to the Cluster Processor. A unit length in x direction corresponds to $10\,ns$, $200\,mV$ in y direction for the LVDS data, and $1\,V$ for the input signal. The zero line is indicated by the number 2 on the left side of the picture.

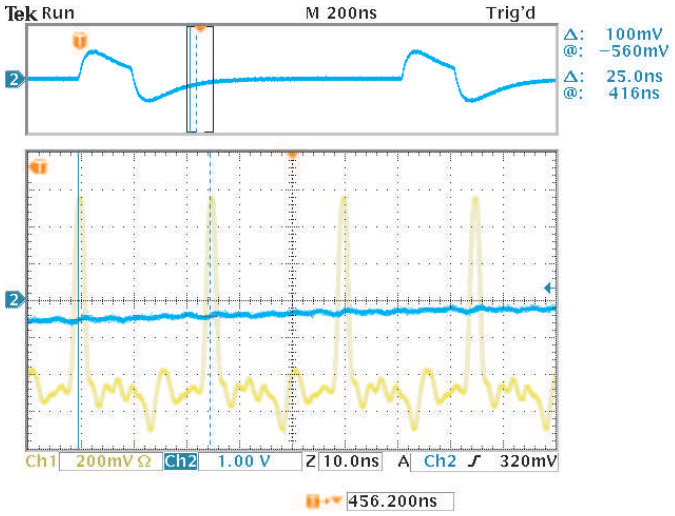

Figure 7.8: Close-up view of the second LVDS output channel that transmits data to the Cluster Processor. All data are zero for both MCM channels. A unit length in x direction corresponds to 10 ns, 200 mV in y direction for the LVDS data, and 1 V for the input signal. The zero line is indicated by the number 2 on the left side of the picture.

7.3 Interpretation of the MCM Real-Time Data

Two test iterations were conducted which both used the same analog pulse as an input to the MCM. All measurements of the real-time LVDS output are summarized in Table 7.2. The deviations between the two LVDS measurements most likely arose because of a different sampling time of the input data: the Phos4 might be in another state due to a power shutdown between the two measurements.

As stated in Section 4.2.2, the two MCM LVDS outputs that provide data to the Cluster Processor transmit two MCM channels each. The first bit of all LVDS real-time data sent to the Cluster Processor is a so-called "odd-parity bit": it is only "1" if an even number of bits are set in the remaining nine bits of the LVDS data word. As one can see in *e.g.* Figure 7.8, it is not set in the case of zero data transmission. This behavior does not conform to the PPrASIC specification and should therefore be considered as an error of the chip. However, it cannot be excluded that this behavior is due to the non-configuration of the PPrASIC. In the case of all measured non-zero data transmissions, the odd-parity bit is set correctly.

The next bit – the"BC-Mux flag bit" – that is transmitted to the Cluster Processor is set according to the following scheme [36]:

- In the first clock cycle, the flag bit indicates which channel is being sent in the current bunch-crossing: 0 → channel 1, 1 → channel 2. Channel 1 takes precedence if both channels contain non-zero signals.

- In the second clock cycle, the BC-Mux bit indicates the bunch-crossing the sent data actually belongs to: 0 → previous, 1 → current. A zero data in this second cycle is always accompanied by the flag bit set to "1".

This bunch-crossing multiplexing cycle, containing two clock ticks, starts whenever either of the two channels contains non-zero data. In Table 7.2, the second clock cycle is indicated by a (2), whereas the first clock cycle is marked as (1). Since the analog pulse was only applied to a single input channel, the results of the Cluster b (1,2) and Cluster a (2) measurements comply with the expectations. The parity and BC-Mux bit of the Cluster a (1) measurements can be explained with the above statements.
The default output format for the Jet/Energy-Sum Processor is the 10-bit sum of the four 8-bit Cluster Processor channels [36]. In this case, no parity bit is inserted. Therefore, the result of the Jet/Energy-Sum channel is predictable: two leading zeros have to be added to the only Cluster channel data that is non-zero. The observed data agree with this prediction in both test iterations.
In addition to monitoring the real-time data with the oscilloscope, they were also transferred to the crate system via twisted pair cables. A code loaded in the XCV300 simply received the real-time data that were successfully deserialized on the LVDS_r CMC and sent it on to the front panel. A set of LEDs plugged onto the Virtex CMC front connectors showed the patterns specified in Table 7.3. A "1" that was successfully transmitted caused a LED to light. The observed patterns for the Jet/Energy-Sum LVDS channel correspond exactly to the ones measured with the oscilloscope. The apparent differences in the Cluster LVDS channels can be understood by applying a logical "OR" to the patterns of the (1) and (2) patterns of a Cluster channel from Table 7.2. This is necessary, since the LEDs are

Iteration	**LVDS channel**	**Parity Bit**	**BC-Mux**	**LVDS Data [LSB...MSB]**
1	Cluster a (1)	0	0	0100_1100
1	Cluster a (2)	0	1	0000_0000
1	Cluster b (1)	0	0	0000_0000
1	Cluster b (2)	0	0	0000_0000
1	Jet/Energy-Sum	-	-	01_0011_0000
2	Cluster a (1)	0	0	1010_0100
2	Cluster a (2)	0	1	0000_0000
2	Cluster b (1)	0	0	0000_0000
2	Cluster b (2)	0	0	0000_0000
2	Jet/Energy-Sum	-	-	10_1001_0000

Table 7.2: Measurements of real-time LVDS data patterns. These data were recorded with an oscilloscope in two separate test iterations. The three real-time LVDS data streams are denoted Cluster a, Cluster b, and Jet/Energy-Sum. The numbers (1) and (2) distinguish the two time frames that provide data originating from two different MCM input channels to the Cluster Processor.

Iteration	LVDS channel	LED Pattern [LSB...MSB]
1	Cluster a	01_0100_1100
1	Cluster b	00_0000_0000
1	Jet/Energy-Sum	01_0011_0000
2	Cluster a	01_1010_0100
2	Cluster b	00_0000_0000
2	Jet/Energy-Sum	10_1001_0000

Table 7.3: Real-time LVDS data pattern as observed with LEDs after transmission to the Virtex CMC. Each "1" that was successfully transmitted caused a LED on the front panel of the Virtex CMC to light.

too inert to switch between ON and OFF fast enough to distinguish the two time frames (1) and (2). Therefore, the observed LED patterns also correspond to the expectations for the Cluster LVDS channels. This optical test proves that real-time LVDS data can be transferred successfully to the XCV300.

7.4 Conclusions of the MCM Tests

All observed bit patterns remained stable over time and were sensitive to the analog input in a way that the two LSBs were switching between 0 and 1 if one slightly altered the input signal *e.g.* by touching the resonance circuit.
It can be concluded from the tests that the ADCs digitize the incoming signal, the PPrASIC BCID algorithm correctly identifies a signal peak and issues a BCID pattern through the LVDS serializers. The real-time data are consistent with each other and comply with the expectations of both the Cluster and Jet/Energy-Sum Processors. Besides the wrong parity bit during transmission of zero data, all tests are in perfect agreement with the specifications of the PPrASIC and the MCM.

Summary and Outlook

This thesis describes the development of a test environment for the ATLAS Level-1 Calorimeter Trigger Pre-Processor which is responsible for handling all incoming calorimeter trigger tower signals. The tasks of the Pre-Processor includes the digitization of the analog input pulses, attribution of a signal to the correct bunch-crossing, transverse energy calibration, readout of trigger data, and the serial transmission of the results to the subsequent trigger processors. The test environment consists of a graphics card, the MCM Testboard, and a set of PCBs.

A commercial graphics card was programmed to emulate calorimeter trigger tower pulses based on data taken during an ATLAS test beam run using production modules of the HEC, hadronic tile, and EMB calorimeters. In order to satisfy the requirements of the test system, over 200 test beam pulses were re-formatted. Tests of the signal generator included linearity measurements of the graphics card voltage output, investigation of crosstalk between the three color channels, and noise evaluation. All crucial parameters (*i.e.* rise time, signal shape, and pulse length) of the graphics card output match the original calorimeter pulse parameters.

The MCM Testboard is a printed circuit board which holds two main components of the final Pre-Processor Module: the Analog Input Board and the MCM. Both modules were tested for the first time. After initial power tests, an onboard generated analog pulse formed the input signal to the test system. An oscilloscope was used to monitor the real-time LVDS output generated by the Pre-Processor ASIC as a response to the input pulse. Except for the wrong parity bit allocation during the transmission of zero data, all observed output bit patterns comply with the expected results in terms of stability, timing, and format.

A set of three PCBs forms the interface between the MCM Testboard and a standard PC: on the one hand it collects data issued by the MCM Testboard and stores them onto permanent storage media, while on the other hand sends configuration data to the MCM Testboard. Each of these boards is equipped with a FPGA which performs all signal processing tasks. Although source codes for two FPGAs were developed to enable VME access to the boards and the implementation of a freely available I^2C master core, several functions (*e.g.* a serial interface to communicate with the PPrASIC) remain to be integrated.

The test environment presented in this thesis constitutes a first compact test system that incorporates final Pre-Processor components. Initial tests show promising results and can therefore be considered as a step towards the so-called "slice test" that in addition to the Pre-Processor involves the Cluster and Jet/Energy-Sum Processors. However, major

efforts are still required to develop software and firmware for the Pre-Processor test system. The slice test is scheduled to take place in Heidelberg during summer 2003. The complete calorimeter trigger is planned to be available *in situ* at CERN in summer 2006 about six months before the beginning of the LHC operation.

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Glossary

AC	Alternating Current
ADC	Analog-to-Digital Converter
ALICE	A Large Ion Collider Experiment
ASIC	Application Specific Integrated Circuit
ATLAS	A Toroidal LHC ApparatuS
BC-Mux	Bunch-Crossing Multiplexing
BCID	Bunch-Crossing IDentification
CERN	Conseil Européen pour la Recherche Nucléaire
CL	Confidence Level
CLB	Configurable Logic Block
CMC	Common Mezzanine Card
CMOS	Complementary Metal Oxide Semiconductor
CMS	Compact Muon Solenoid
CP	Charge conjugation and Parity
CPLD	Complex Programmable Logic Device
CSC	Cathode Strip Chamber
CTP	Central Trigger Processor
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition System
DIN	Data IN
DOUT	Data OUT

DPRAM	Dual-Ported Random Access Memory
EMB	ElectroMagnetic Barrel
FIFO	First-In-First-Out
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
GUT	Grand Unified Theory
HDL	Hardware Description Language
HEC	Hadronic End Cap
I^2C	Inter-Integrated Circuit
IOB	Input/Output Block
LEP	Large Electron Positron collider
LFAN	LVDS Fanout
LHC	Large Hadron Collider
LHCb	LHC beauty experiment
LSB	Least Significant Bit
LUT	Look-Up-Table
LVDS	Low Voltage Differential Signaling
MCM	Multi-Chip Module
MDT	Monitored Drift Tube
MSB	Most Significant Bit
PAR	Place-And-Route
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
PPM	Pre-Processor Module
PPrASIC	Pre-Processor Application Specific Integrated Circuit

PPrMCM	Pre-Processor Multi-Chip Module
PS	Proton Synchrotron
QCD	Quantum ChromoDynamics
QED	Quantum ElectroDynamics
RAM	Random Access Memory
RemFPGA	Readout Merger Field Programmable Gate Array
ROB	Read-Out Buffer
ROD	Readout Driver Module
ROI	Region Of Interest
RPC	Resistive Plate Chamber
SCL	Serial Clock
SCT	SemiConductor Tracker
SDA	Serial Data
SMD	Surface Mounting Device
SPI	Serial Peripheral Interface
SPS	Super Proton Synchrotron
SRAM	Static Random Access Memory
SUSY	SUperSYmmetry
TGC	Thin Gap Chamber
TRT	Transition Radiation Tracker
TTC	Trigger and Timing Control system
VCO	Voltage Controlled Oscillator
Verilog	Verifying Logic
VHDL	Very high speed integrated circuit Hardware Description Language
VME	Versa Module Eurocard

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