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Initial Tests of the ATLAS Level-1 Trigger Pre-Processor

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Erste Tests des ATLAS Level-1 Kalorimeter Trigger PräProzessors:

Diese Arbeit beschreibt erste Tests des Level-1 Kalorimeter PräProzessors unter ATLAS Bedingungen. Der PräProzessor verarbeitet analoge Kalorimeter Pulse und liefert digitale kalibrierte Werte, die der im Kalorimeter abgegebenen transversalen Energie entsprechen.

Da er damit auf der Grenze zweier grundverschiedener Bereiche liegt, stellt die Integration des PräProzessors in die Atlas Trigger Kette besondere Herausforderungen. Zu Beginn wurde ein Testsystem und später Prototypen finaler Module eingesetzt, um die Funktionalität des PräProzessors und der Schnittstellen der Systeme vor und nach ihm in der Signalkette zu überprüfen. Zuerst wurden Labortests durchgeführt, die den Bereich von speziellen Tests einzelner Schnittstellen bis hin zum Aufbau der gesamten digitalen oder analogen Kette umfassten. Sie wurden durch einen gemeinsamen Testbeam Einsatz des gesamten Level-1 Triggers mit allen ATLAS Detektorarten am CERN zusammengefasst.

Die nachfolgende Arbeit beschreibt den Aufbau, die Durchführung und die beteiligten Systeme aller Tests. Hierbei liefern die vorgestellten Ergebnisse eindeutige Hinweise das der PräProzessor in der Lage ist seine Aufgaben, den Anforderungen genügend, zu erfüllen.

Initial Tests of the ATLAS Level-1 Trigger Pre-Processor:

This thesis describes initial tests of the Level-1 Calorimeter Trigger Pre-Processor in the ATLAS environment. The Pre-Processor processes analog calorimeter pulses and provides digital, calibrated values corresponding to the amount of transversal energy deposited in the calorimeters.

As it thus lies on the border of two different realms integration of the Pre-Processor into the ATLAS trigger chain poses various distinctive challenges. Initially using a test system and then prototypes of final modules, combined functionality and interfacing with the predecessors and successors of the system in the signal chain were first verified in laboratory experiments. They spanned from custom interface tests of two modules to realistic full setups of the digital processing or analog signal chain. These steps to join the different systems together and achieve proper functioning were summed up in a combined ATLAS test beam at the CERN, with all ATLAS detector types and the full Level-1 Trigger participating.

All systems, setups and tests are described in the following, the results strongly evidencing that the Pre-Processor is able to fulfill its tasks and comply with its requirements.

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Chapter 1

Introduction

Since the birth of modern science at the dawn of the 17th century its goal was to find the underlying fundamental principles of phenomena experienced in our world. Its most influential early achievement was the Philosophiae Naturalis Principia Mathematica published by Isaac Newton in 1687. This work not only presented the basic principles of the movement of all bodies, but also was hereby able to unify the force seemingly dominating our everyday life, the gravitation on Earth, and the rules of the movement of celestial bodies.

More than three centuries later our theories on particles and their interactions have become much more refined but also more estranged from our everyday experiences, often even contradicting expectations derived from observations of our macroscopic environment. In high energy physics scenarios, at an inconceivably small scale, the Standard Model is well established as the leading theory describing all fundamental particles and their interactions. Yet it does neither include gravity nor is able to explain the origin of inertia or mass, which have historically been the first phenomena to be investigated by humankind. Additions to the Standard Model have been in discussion for several decades, though, the most firmly settled explanation of particle masses being the Higgs mechanism with its Higgs boson, devised in the 1960s by Peter Higgs, yet clear evidence for its existence is still missing.

But in the year 2007 a new collider experiment, the Large Hadron Collider at CERN, will starts its operation and produce collisions of proton beams with an unprecedented energy and luminosity. The ATLAS project, one of the detectors in the LHC, will among other things attempt to finally put this last missing piece of the Standard Model into place. While it is generally believed that the Higgs boson will certainly make its appearance at the LHC, detecting and identifying it will be all but trivial. A highly efficient trigger system will be needed to select the minuscule amount of promising events out of the huge background for storage and offline analysis.

ATLAS uses an approach of three trigger stages for event selection, the fast and powerful Level-1 hardware trigger being the first stage. The requirements to the ATLAS Level-1 trigger are quite demanding, but a feasible design has been found and was verified using conceptual modules performing the trigger operations on a small scale in 1998. Since then its subsystems have been developed and tested individually. With the start of the experiment coming closer and the commissioning of the Level-1 Trigger nearing, tests to join them together have become a high priority. These tests, starting humbly with setups of test system to verify single interfaces and reaching a climax with a combined run at the test beam at CERN, are the subject of this thesis.

Chapter 2 introduces the LHC and the ATLAS experiment in general, including physics scenarios. Chapter 3 gives an overview of the ATLAS Trigger System, with a focus on the Level-1 Calorimeter Trigger. An introduction of the strategy to collect evidence for a working system including most foremost the Pre-Processor can be found in chapter 4, while the chapters 5 through 7 describe the actual experiments and their results. The last chapter summarizes the achievements and provides an outlook.

Chapter 2

The ATLAS Experiment at the Large Hadron Collider

2.1 The Large Hadron Collider at CERN

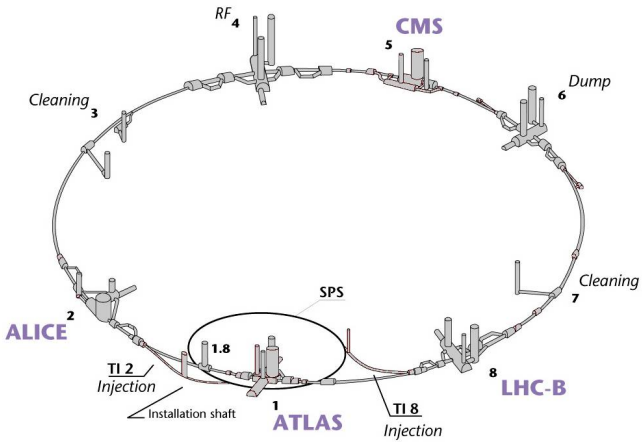

Figure 2.1: Layout of the LHC, including access points[1]

The Large Hadron Collider (LHC), currently being built in the former LEP tunnel at the European Organization for Nuclear Research (CERN) site near Geneva, Switzerland, is an accelerator which will primarily bring protons, but heavy-ion(Pb) operation is also planned, into head-on collisions at unprecedented energies.

Bunches of protons, each containing about 10^{11} particles, are accelerated and stored in two separate counter-rotating circular beams, reaching an energy of 7

TeV each. Collisions occur at four interaction points, where the beamlines cross. The general purpose experiments ATLAS[1] and CMS[2] occupy two of these points, ALICE[3] and LHCb[4] the other two.

In order to allow for a large discovery potential of these experiments, high energy in the center-of-mass system is needed. With the beam energy of 7 TeV, the center-of-mass energy $\sqrt{s}$ of a proton-proton collision is 14 TeV. Only a fraction of this energy ($\sim$0.1) can be used to create new particles, though, as the colliding partners are partons of the protons, carrying only a portion of the energy. In contrast to electron-positron colliders the limiting factor of the beam energy is the ability to keep the particles on track, the inventive superconducting dipole magnets with magnetic field strength up to 8.33 T along the beamline being one of the major engineering challenges of the LHC.

To get a high rate of interesting physics events and thus to utilize the discovery potential an extremely high luminosity, the number of particles crossing a unit area per time, is essential. The first way to achieve this goal is having tight proton bunches with a large number of particles. Certain limits exist, like the repulsive force between protons, widening the bunches for example at the interaction points where the particle density is exceptionally high. Thus to achieve the luminosity goal of the LHC, at first a luminosity $\mathcal{L} = 10^{33} cm^{-2} s^{-1}$ (to be later increased by a factor of 10), a large number of bunches in the beam is also needed. Roughly three thousand[5] bunches are stored, together with the speed very close to the speed of light ($v \approx 0.999999991c$) and the circumference of 27km resulting in collisions occurring with a frequency of 40 MHz. At high luminosity an average of about 23 interactions will take place in each bunch-crossing every 25 ns, resulting in up to 10.000 tracks observed within 100ns, the typical duration of electronic signals in the detectors. The challenge of the LHC experiments is to identify and select the interesting physics events out of this so-called 'pile-up' background at the required rate. High granularity of the detectors, fast signals and powerful trigger systems are required for this task.

2.2 The ATLAS Detector

ATLAS is a general purpose experiment at the LHC, currently being built by a collaboration of about 150 institutes with more than 1500 physicists. ATLAS was designed to cover a large spectrum of LHC physics, most foremost searches

[1] A Toroidal LHC ApparatuS
[2] Compact Muon Solenoid
[3] A Large Ion Collider Experiment
[4] Large Hadron Collider beauty experiment
[5] plus 600 empty bunches due to the LHC bunch structure

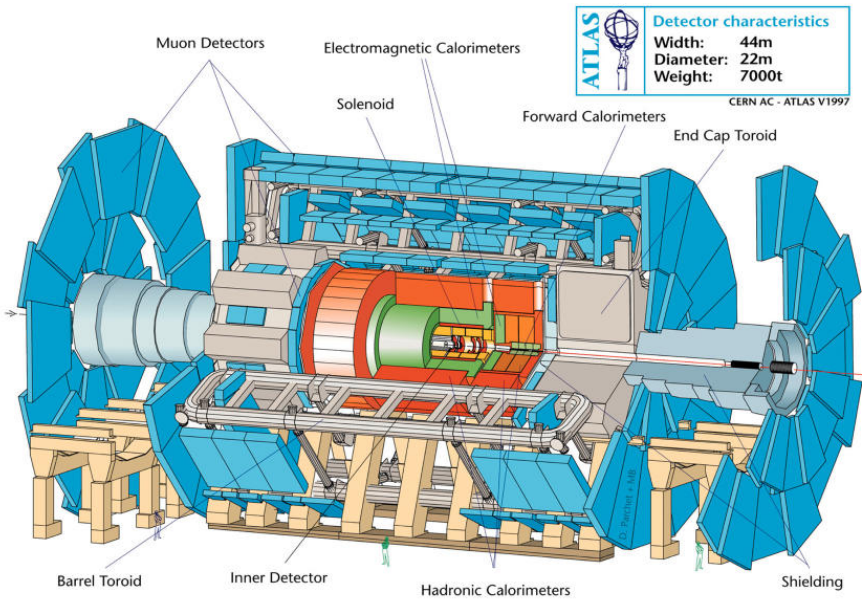

Figure 2.2: Schematic of the ATLAS detector

for the Higgs Boson, alternative schemes for the spontaneous symmetry-breaking mechanism and searches for supersymmetric particles, new gauge bosons, leptoquarks, and quark and lepton compositeness indicating extensions to the Standard Model and new physics beyond it[2]; but also high precision measurements of for example quark masses and decay properties.

The ATLAS approach to LHC measurements is very precise electromagnetic calorimetry complemented by full coverage hadronic calorimetry, high precision muon momentum measurement with huge air-core toroids and an efficient tracking system. A large acceptance in pseudorapidity[6] η with full coverage of the azimuthal angle[7] ϕ and a very powerful, highly efficient trigger system provide excellent efficiencies for most interesting physics events at the LHC.

The ATLAS detector consists of three subdetectors: the Inner Detector, the Calorimetry and the Muon System(listed outwards from the point of interaction).

[6]the rapidity is defined as $Y = \frac{1}{2} ln \frac{E+p \cdot cos\phi}{E-p \cdot cos\phi}$ and Lorentz-invariant, the pseudorapidity is an approximation of Y if momentum or mass of a particle are unknown; for $\beta \to 1$ the pseudorapidity equals $\lim_{\beta \to 1} Y$, both being $-\ln tan \frac{\theta}{2}$, where θ is the polar angle

[7]measured around the beam axis

2.2.1 Inner Detector

Surrounded by a solenoid magnet with an axial magnetic field of 2 T, the inner detector's tasks are to reconstruct tracks and vertices with high efficiency as well as provide particle identification. The inner detector consist of three layers and covers the range from $\eta = -2.5$ to $\eta = 2.5$.

Semiconductor pixel detectors form the innermost layer closest to the interaction point, their very good resolution allowing to determine whether a track originates from the primary proton-proton collision or from a decay process following it. The next layer consists of silicon microstrip detectors and supplements the track reconstruction with further high precision space points. Outermost the Transition Radiation Tracker, a continuous straw tube detector, provides data for robust pattern reconstruction and particle identification.

The Inner Detector as a whole has to be radiation hard, have a very fine granularity and good momentum resolution, without bringing too much material into the area around the interaction point, else its own momentum resolution and the energy measurement in the calorimeters would be degraded.

2.2.2 ATLAS Calorimetry

The ATLAS calorimetry approach is twofold, matching its goals as a general purpose detector. An electromagnetic calorimeter is used for electron and photon identification and measurements, a hadronic calorimeter for precise jet, isolated hadron and missing transverse energy measurements. Both calorimeters have 'barrel'[8] sections to cover the central η region, as well as 'end-cap' modules for the outer η regions to reach a very good coverage up to $\eta = 3.2$. Forward calorimeters around the beamline, in an extremely intense radiation environment, extend that even further to η up to 4.9.

Due to the pileup[9] caused by the high event rate, a fine granularity as well as a fast response are vital for all calorimeters, even more so as they will be the key component for many measurements in interesting physics channels. Given the particle flux, radiation hardness is also an issue and is achieved with all detector modules in various ways according to local geometry and requirements.

Electromagnetic Calorimeter

The electromagnetic calorimeter is a heterogenous shower counter[10], using a basic approach of liquid Argon gas(LAr) as sensitive material and lead as absorber,

[8] cylindrically shaped around the beamline

[9] background signals adding to observed events

[10] also called Sampling Calorimeter, as only a small fraction of the shower energy is 'sampled' in the sensitive material

intrinsically resulting in radiation resistance. To achieve seamless ϕ coverage the Electromagnetic Barrel and Endcap Calorimeters have an 'accordion' geometry, formed by stacked zigzag shaped lead absorbers with LAr gaps and an electrode structure in between. The calorimeter is preceded by an integrated preshower detector and a separate presampler to preserve the energy and direction resolutions despite of the cryostat and solenoid material in front of it.

The total thickness of the Electromagnetic Calorimeter is 25 radiation lengths X_0[11], thus containing the majority of the electrons and photons. The total number of channels is $\sim 200,000$.

Hadronic Calorimeter

To detect and measure hadrons passing the Electromagnetic Calorimeter with only small energy losses, it is surrounded by the Hadronic Calorimeter. Complying to local requirements, this calorimeter uses different technologies in the barrel and endcap regions. The barrel region is covered by the TileCal Barrel and two TileCal Extended Barrels. These are analogously built sampling calorimeters with scintillating tiles embedded in an iron absorber matrix. The Hadronic End Cap Calorimeter makes use of the same LAr technology as the Electromagnetic Calorimeter, but using copper as absorbing material. The total amount of channels in the Hadronic Calorimeter is about $21,000$.

Forward Calorimeter

The Forward LAr Calorimeter, closest to the beamline and thus subject to an extreme particle flux, is built using a metallic tube and rod electrode structure embedded in copper(inner section) or tungsten with a very small LAr gap. It covers the full ϕ range and $|\eta|$ up to 4.9. The Forward Calorimeter is both used for electron/photon and isolated hadron/jet detection and measurements, and has roughly 11,000 readout channels.

2.2.3 Muon System

The outer frame of the ATLAS detector is dominated by its Muon Spectrometer including the huge superconducting air-core toroid magnets, as precise muon measurements and triggers are needed to utilize the promising discovery potential of physics channels with high energy final state muons[12].

The strong toroidal(around the beamline) magnetic field curves the muon tracks allowing to measure their energy and charge. This is done using Cathode

[11] X_0 is the thickness of material over which electron energy is reduced to a fraction of 1/e

[12] f.e. the Higgs decay $H \rightarrow ZZ^* \rightarrow 4\mu$

Strip Chambers in the endcaps, where the radiation levels are high, and with Monitored Drift Tubes in the barrel region. Further coordinate measurements for track reconstruction and muon triggering are provided by Resistive Plate Chambers in the barrel and Thin Gap Chambers in the endcaps.

2.3 ATLAS physics issues and resulting trigger requirements

2.3.1 The LHC as a high-energy physics laboratory

Bunches of protons counter-rotate in the LHC with an energy of 7 TeV each. As they collide head-on under a negligible angle, the center-of-mass energy $\sqrt{s}$ of a proton-proton collision is 14 TeV. But as the protons' partons can be considered free particles at these energies and the timescale of the interaction, typically only about 1/10 of this energy is available for production of new particles through a parton-parton interaction. For this reason LHC physics is often called TeV physics, indicating physics scenarios with $\sqrt{s} \approx 1$ TeV.

As the total cross-section of an inelastic proton-proton collision is quite large at LHC energies, combined with the high luminosity more than twenty events can occur in a single bunch-crossing. The huge amounts of data to be processed and difficulties to identify a certain event in the pileup background of all others therefore make triggering for interesting physics events in ATLAS challenging. Elastic proton-proton scattering at low angles additionally imposes high radiation requirements on detector components close to the beam line.

Concerning the LHC energy, it is quite possible that the Standard Model, the current theory of fundamental particles and their interactions, is valid for the whole or most of the energy scale, making it the most firmly settled theoretical background for LHC events. The Standard Model originated in the 1970s and is unsurpassed in precise predictions for the outcome of a wide spectrum of experiments since then. Today all but one parts of the Standard Model are very well established, that part being the mechanism bestowing masses unto the particles. These masses, as well as other aspects like the existence of the three 'families' of fundamental particles, have currently to be taken as granted and can not be derived from the theory. Proposals have been made, though, most prominently the Higgs mechanism for the problem of the masses, which will have to be tested by experiments like ATLAS.

The Standard Model is a long standing triumph of high-energy physics, not being contradicted by experimental data yet, but the search for extensions or

alternatives is always on[13].

The Standard Model of particle physics

The Standard Model is a theory that describes all fundamental particles and their interactions and orders them into groups. Only a quick overview will be given in this chapter, more detailed descriptions can be found elsewhere(f.e. [3]). The Standard Model does not include gravity, being negligible in high-energy physics scenarios.

The fundamental particles of the Standard Model fall into two groups: half-integer spin fermions(matter particles) and force carrying bosons with an integer spin. An antimatter partner of the same mass and opposite charge is assigned to all particles.

	Families		
	I	II	III
Quarks	up down	charm strange	top bottom
Leptons	e^- ν_e	μ^- ν_μ	τ^- ν_τ

Table 2.1: Fermions in the Standard Model

The fermions can be further ordered into two groups: quarks, which are the building blocks of all hadrons and are subject to the strong force, and leptons together with their neutrinos. While three families of each of these exist, all 'normal' matter is built using only the first family. The reason for the existence of the other families is unknown[14].

Interaction	Force Carriers	Acting on
Strong	Gluon(g)	color charge
Electromagnetic	Photon(γ)	el. charge
Weak	$Z^0, W^\pm$	weak charge

Table 2.2: Fundamental forces and their bosons

[13]some may say the most disappointing thing about the Standard Model is that it hasn't been contradicted yet

[14]I.I. Rabi on the discovery of the muon: 'Who ordered that?"

The Standard Model also describes the fundamental forces acting between the particles and the bosons exchanged in the interaction, using gauge theories: The electroweak theory introducing the W and Z bosons as carrier particles of the weak force and the photon as mediator of electromagnetic interactions[15], and the strong force based on the color exchange of quarks and gluons.

The Higgs Boson

One single piece is still missing in the jigsaw puzzle of the Standard Model, the mechanism bestowing masses unto all particles. The simplest solution to the mass problem in the Standard Model is one with all masses being zero, definitely contradicting common experience and experimental results.

The most elegant solution to actually get fundamental particles with mass is the Higgs mechanism. A fourth field is added to the Standard Model, its most prominent features being that it affects all particles and its lowest energy state is not zero. You end up with the Higgs field permeating all of space and, as a simple model, can be considered having a direction in a non spacial coordinate. Looking at the electroweak bosons, the photon would be a boson traveling along that direction, unhindered with its natural speed(the speed of light) and no mass. The W and Z bosons would be bosons traveling in the other direction, needing to constantly 'flip' the field getting masses and inertia in the process.

Leaving the simple model, the symmetry-breaking mechanism of the electroweak interaction predicts a new spin 0 boson, which could be the Higgs. The number of Higgs bosons could be higher, though, and even a Higgs mechanism without a boson is not inconceivable. The mass of the Higgs boson can not be theoretically predicted, but unitary arguments, requirements of the stability of the electroweak vacuum and the validity range of the Standard Model imply certain bounds. These bounds are highly dependant on specific assumptions, though, and including most sensible possibilities the Higgs mass could be anywhere between 50 and 800 GeV.

The total Standard Model Higgs boson production cross-section at the LHC has various contributions, most foremost gg and WW fusion, and it is searched for in several decay channels in ATLAS:

- $H \rightarrow \gamma\gamma$
- $H \rightarrow \overline{b}b$
- $H \rightarrow ZZ^* \rightarrow 4l$

[15] despite the historical name the weak interaction has comparable relative strength to the electromagnetic one in high-energy physics situation with an energy in the order of the mass of the weak bosons

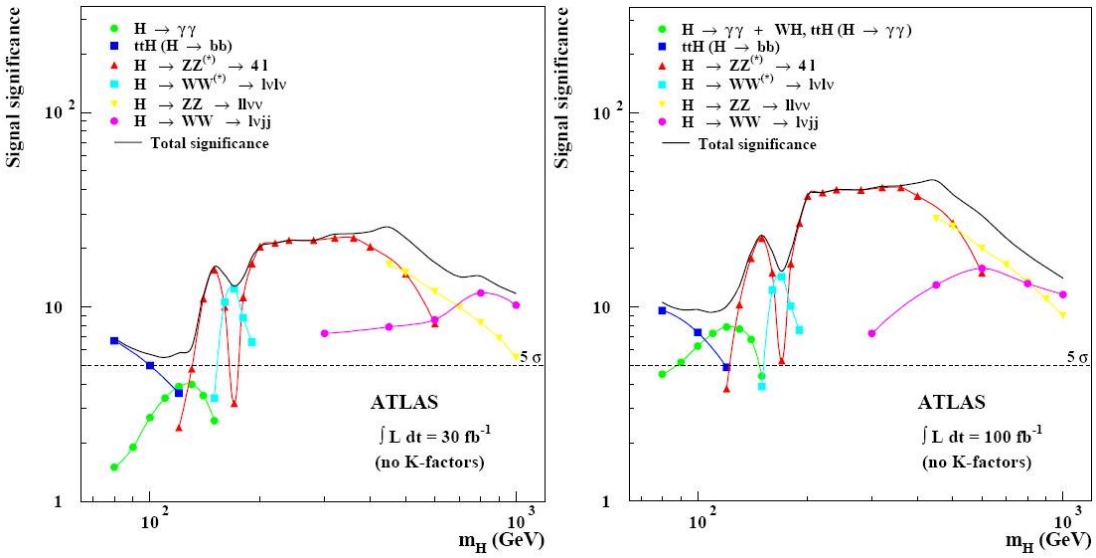

Figure 2.3: Statistical Significances for the discovery of a Standard Model Higgs at ATLAS depending on the Higgs mass, for two accumulated luminosities[4]

- $H \rightarrow ZZ \rightarrow 4l$ and $H \rightarrow ZZ \rightarrow ll\nu\nu$
- $H \rightarrow WW \rightarrow l\nu jj$ and $H \rightarrow ZZ \rightarrow lljj$
- $H \rightarrow WW^* \rightarrow l\nu l\nu$

These channels impose various requirements onto the detector and trigger. At first of course oustanding general energy and angular resolutions of the detector and among others also excellent charged lepton momentum resolution and identification are needed on all levels, including the trigger, plus a close to hermetic coverage of η/ϕ space for channels including νs.

Beyond the Standard Model

Above the validity range of the Standard Model was used as one restraining factor of the Higgs mass. In detail the Higgs mass must be below 800 GeV if the Standard model holds true up to 1 TeV, the characteristic center of mass energy of a parton-parton interaction at the LHC. That means it would be possible for the Higgs to have a higher mass, but then the LHC would reveal new physics, beyond the Standard Model[16].

[16]as either the Higgs mass or the energy to expect new physics are in the LHC range, its a win-win situation

Supersymmetry(SUSY) is the best motivated of these extensions to the Standard Model. In supersymmetric theories, each fermion has a supersymmetric partner boson, and vice versa. If SUSY exists at the 1 TeV scale, the discovery of supersymmetric particles at the LHC can be expected. The lightest supersymmetric particle is thought to be stable and weakly interacting, resulting in signatures with large missing transverse energy E_T^{miss}.

One other possible extension is the technicolor theory, which propagates a more dynamic electroweak symmetry breaking and assumes the existence of technifermions carrying technicolor charge.

Moreover while physics at current energies use three spacial and one time coordinates, there are expectations of extra dimensions becoming accessible at the LHC energy scale.

Heavy quark and lepton physics is another area that will be under study at the LHC, with the possibility of discovery of a fourth family of fundamental particles.

Precision measurements

In addition to new physics, known physics phenomena will also be probed and measured at ATLAS. B Physics is one of these, with an emphasize on the nature of the CP violation in B-meson decays.

Additionally the LHC will be an excellent place to test predictions of QCD[17] and establish additional constraints, as well as measure f.e. the strong coupling constant.

2.3.2 Trigger Challenges

ATLAS will conduct all the above searches and measurements, most prominently including the one for the Higgs boson. As the production cross sections of sought after particles are minuscule compared to the total inelastic cross section of a LHC proton bunch collision, stringent requirements for trigger efficiencies have to be met(see figure 2.4 on page 13).

The rate of inelastic proton-proton interactions at the LHC is of the order of 1 GHz, the input rate of the trigger is of course 40 MHz, the bunch-crossing frequency. The difference of these two numbers results from the average number of events per bunch-crossing being significantly larger than 1($\sim$23 at high luminosity). These events can naturally not be separated before the trigger, only the prerequisites to single them out, a high granularity and excellent tracking, are provided. Furthermore the typical time of an electronic signal from the detector

[17]Quantum chromodynamics, the theory of the strong interaction

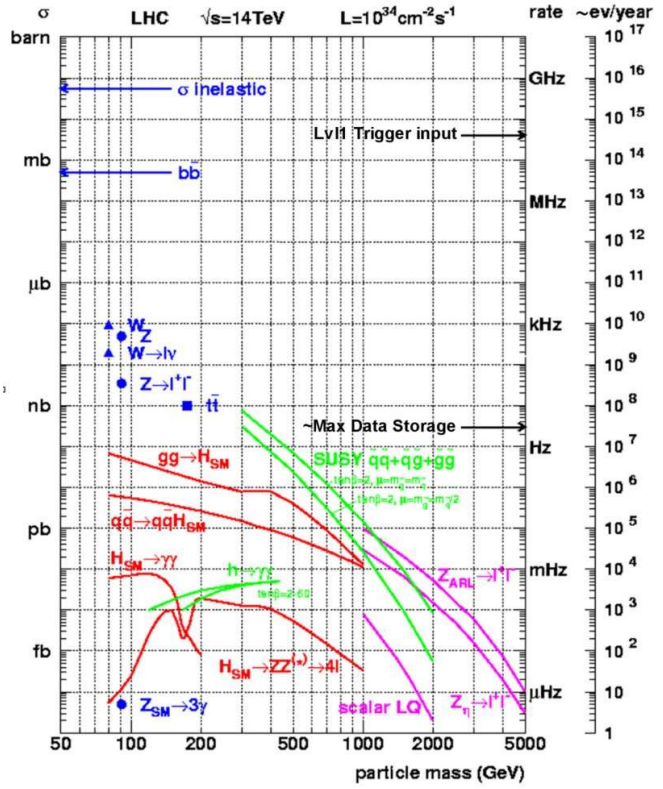

Figure 2.4: Cross-sections and event rates at the LHC

is much longer(∼100ns) than a bunch-crossing(25ns), so a high granularity is also essential to keep the occupancy of single trigger channels low.

Events can only be stored at a rate of less than 100 Hz, still resulting in huge amounts of data as one event has about 1 MByte. As a consequence the trigger has to lower the event rate by about seven orders of magnitude. Without a highly efficient trigger events in interesting physics channels could not be identified among the pileup background, or be lost due to the limited data processing and storing capabilities.

On figure 2.4 one can also see that f.e. the $b\bar{b}$ production rate is very high, only allowing the selection of very few of these for B-physics studies, so strict trigger selection is also inevitable in that field. Generally the interaction rate is too high to simply select all high E_T events like one could do in a lepton collider experiment, and more sophisticated and selective algorithms are required.

Chapter 3

The ATLAS Trigger System

The ATLAS trigger system is designed to overcome two major challenges. The first requirement for the trigger system is excellent efficiency, reducing the event rate by seven orders of magnitude(see section 2.3.2 on page 12). The second one is latency. As only the events tagged for final storage can be saved on disk due to the huge amounts of data, the detector readout has first to be temporarily stored in buffers, allowing the trigger some time to reach an online realtime decision. The total buffer size is of course limited and thus the length quite restricted by the amount of data needed to be held.

The ATLAS reply to these demands is a three-level trigger and data acquisition system. At the first level a hardware trigger reaches a huge reduction in event rate in a very short time, locally searching for signatures of high energy muons, electrons, photons, jets and isolated hadrons as well as global trigger objects like large missing transverse energy. The second level trigger selects candidates for interesting physics events mostly using the information and regions of interest supplied by the first level, while at the third level an event filter accesses full event data like one would do for offline analysis.

3.1 Overview over the Trigger System

40 Million bunch-crossings occur at the LHC every second, that is one every 25ns. As the event data of each amounts to about 1 MByte, less than 100 of these can be recorded for off-line analysis. Consequently a decision to keep or dump an event has also to be made every 25ns. As it is not possible to reach such a decision inside this time interval, all signals from the detectors are first stored in a Pipeline-Memory with a length of $2.5\mu s$ and then preselected ones in Readout Buffers. This buys some time for the individual decisions, nonetheless the rate at which decisions are needed stays the same. The solution to solve

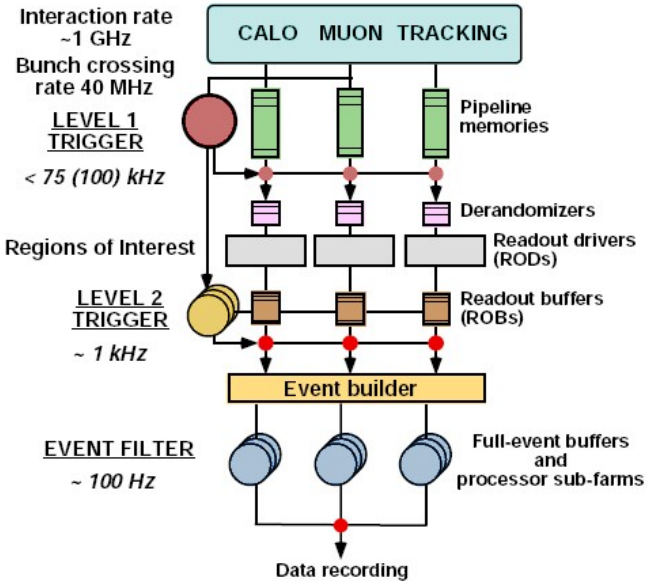

Figure 3.1: Block diagram of the ATLAS Trigger/DAQ system[8]

this problem in ATLAS is massive parallel processing, f.e. naturally achieved at Level-1 by a hardware trigger.

3.1.1 Level-1 Trigger

The first level trigger already significantly reduces the event rate to less than 100kHz. It searches for trigger objects hinting at interesting physics events, f.e. high energy lepton, jet or isolated hadron candidates using calorimeter and muon system data. These are found locally and then global multiplicities of objects passing certain thresholds are calculated. Additionally some large trigger objects like total transverse energy(E_T^{total}) and missing transverse Energy (E_T^{miss}) in the calorimeters are computed. By comparing all this data to a trigger menu a decision is made whether to keep an event, in which case a Level-1 Accept signal is sent to the detector to read out the full event from the Pipeline Memories. Event data not read out in time is automatically lost.

To be able to readout the correct data in the first place, another vital task of the Level-1 trigger is identifying the correct bunch-crossing correlating to the event. This is a non trivial task due to the short bunch-crossing interval of 25ns. In the Muon Spectrometer the time-of-flight is of that order, and calorimeter pulses extend over several bunch-crossings.

As the Pipeline Memory length is fixed and a large cost factor, measured

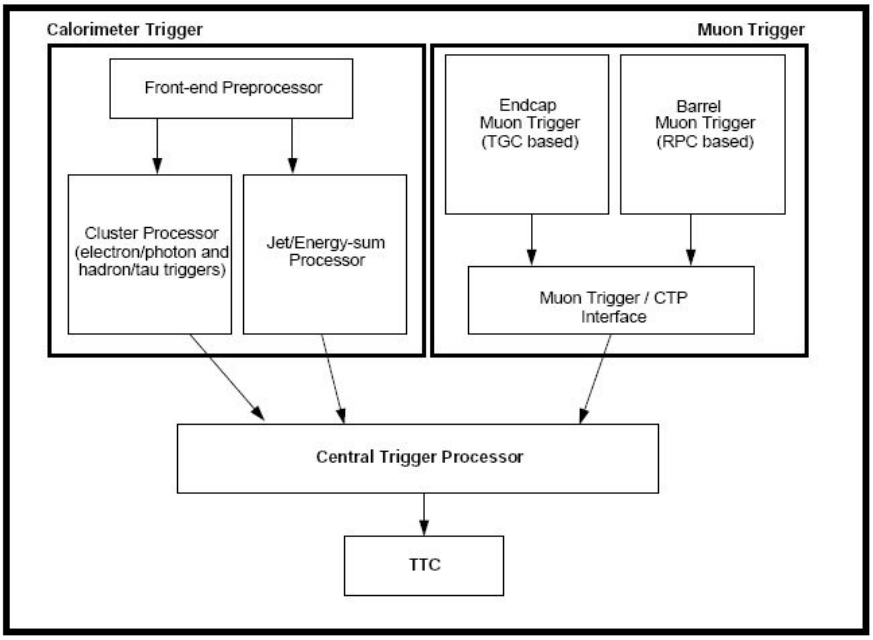

Figure 3.2: Block diagram of the LVL1 trigger system[8]

from the time of the proton-proton collision to the arrival of the Level-1 Accept no more than $2.5\mu s$ may pass. The latency goal of the Level-1 Trigger is $2\mu s$ to retain some contingency reserve. In order to achieve this goal a system of purpose-built hardware processors is used.

The Level-1 Trigger consists of three subsystems: the Calorimeter Trigger, the Muon Trigger and the Central Trigger Processor.

Calorimeter Trigger

The Level-1 Calorimeter Trigger receives analog input from all ATLAS calorimeters. As about 230,000 channels are provided, the granularity has to be reduced at trigger level to be able to build a feasible system. Up to 60 calorimeter channels are summed into so called trigger-towers, resulting in $\sim$7200 analog input channels into the calorimeter trigger, having a typical granularity of 0.1×0.1 in η/ϕ. The signals are transmitted to the trigger via twisted pair cables with a length of up to 70m, as the trigger system is not housed in the detector cavern.

The trigger-tower signals are digitized in the Pre-Processor and the transversal energy E_T is extracted and assigned to the correct bunch crossing. In the further fully digital system, a subsystem called Cluster Processor searches for local energy deposition hinting at high-E_T electrons/photons and hadrons/taus.

The full trigger-tower granularity is used.

A second subsystem, the Jet/Energy-Sum Processor, searches for high-E_T jets and computes the E_T^{miss} vector and total scalar E_T in parallel to the Cluster Processor. This is done using further reduced granularity, with sums of four trigger-towers as unit.

All finds and the global E_T sums are compared to thresholds(f.e. jets with $E_T > 90GeV$), and the numbers of trigger objects passing these thresholds are sent to the Central Trigger Processor. In case of a Level-1 Accept the objects and their coordinates are also sent to the Region-of-Interest Builder(RoIB), which is the interface to the Level-2 Trigger, and made available to the Data Acquisition system to document the trigger decision.

As the subject of this thesis are tests of the Level-1 Calorimeter Trigger, more information on this system and its subsystems is given in section 3.2 starting on page 20.

Muon Trigger

The muon trigger receives precise and fast information about hits in the muon Trigger chambers, which are Resistive Plate Chambers in the barrel region of the detector and Thin Gap Chambers in the endcaps. As more than 800,000 input channels are generated, only part of the muon trigger is in the trigger cavern USA15, the rest being built into front-end electronics on the detector to reduce the number of transmitted channels and thus the amount of cabling to the shielded USA15.

Mirroring the use of the different detector types in the barrel and endcap regions, the muon trigger is divided into 2 parallel subsystems. Both search for hit patterns indicating high-p_T muons originating from the interaction region, and additionally low p_T muon triggering is envisioned to be used in low luminosity runs. The muon trigger has sufficient time resolution to identify the bunch-crossing in which a muon originated with a very high probability.

A third subsystem bundles and combines the data from the two triggers and acts as an interface to the Central Trigger Processor. In the case that an event is accepted for readout it also sends Region of Interest(RoI) information to the Level-2 Trigger.

Central Trigger Processor

The Central Trigger Processor(CTP) receives the multiplicities of muons, electron/photons, hadrons/taus and jets passing the thresholds in the other processors, plus the thresholds passed by the global E_T sums and combines all that data in order to reach an overall Level-1 decision. The decision is made by comparing

the input data to a trigger menu, which consists of up to 96 trigger items. Each of these trigger items can be a combination of different inputs, f.e. one muon with $p_T > 10GeV$ together with an isolated EM cluster with $E_T > 15GeV$.

Basically, if any trigger item is matched by the data a Level-1 Accept is generated, though the different trigger items can be individually prescaled to lower high trigger rates. Moreover the CTP handles deadtime control for the Level-1 Trigger, the most basic function being that no two Level-1 Accepts can occur in a quick succession, typically no less than 4 bunch-crossings are allowed in between.

If an event is accepted by the CTP, a Level-1 accept is send to the Pipeline Memories to initiate readout of the full event data into Readout Buffers where it awaits a Level-2 decision, and to the Level-1 subsystems. These make the RoI data available to the Level-2 trigger and supply data documenting the decision process to the Data Acquisition system.

3.1.2 High Level Trigger

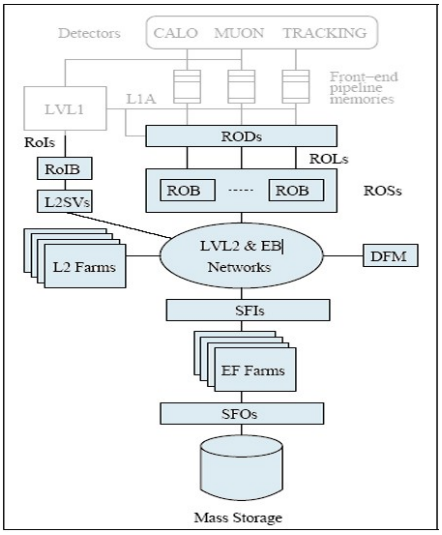

Figure 3.3: Principal components of the High Level Trigger and DAQ[5]

High Level Trigger is a collective name for the level-2(LVL2) trigger and the event filter(EF). Both are software triggers using PC farms, and an integral part of the Data Acquisition(DAQ) system. They differ in their approach, though, to achieve maximum combined efficiency. The LVL2 trigger uses fast, limited precision algorithms with a high rejection factor needing only modest computing power. Consequently it is able to concurrently process events with a high rate.

The event filter uses high precision algorithms on the full event data, using up more extensive computing resources, and thus only being able to operate on a smaller number of events and a much lower rate. The High Level Trigger selection algorithms are developed in the offline Athena environment.

Level-2 Trigger

The Level-2 Trigger is the subsystem of the High Level Trigger receiving data directly from Level-1. Therefore it is required to run with the high Level-1 Accept rate of up to 100kHz. It should also take no more than ∼10ms to reach a decision, as the full event data has to be stored in Readout Buffers(ROB) in the meanwhile. The Regions of Interest from the different Level-1 subsystems are first combined in the Regions-of-Interest Builders(RoIB). These then pass the data to the LVL2 Supervisor (L2SV) which assigns the event to one of the processors of the L2 Farms. The selection algorithms running on those request fractions of the full event data from the ROBs, typically only ∼2% centered around the RoI coordinates. Several algorithms are run sequentially to refine the trigger decision and an event can be rejected at each stage. The final LVL2 trigger decision is sent back using the L2SV to the Data Flow Manager(DFM), which initiates either event building or deletion.

Event Filter

The Event Filter(EF) Farms receive fully built events from the Sub-Farm Inputs(SFI), allocating them to single processors. At the EF stage the available tools, algorithms and information closely resemble offline analysis, and a thorough final decision is made. In contrast to Trigger Levels 1 and 2 the data is not buffered during the decision making but only resides inside the EF memories. Accepted events are transmitted to Mass Storage via the Sub-Farm Output(SFO).

3.2 The ATLAS Level-1 Calorimeter Trigger

The ATLAS Level-1 Calorimeter Trigger(L1 Calo Trigger) directly receives analog data from the calorimeters at a rate of 40MHz [1]. As the number of channels received from the calorimeters is about 230,000, the granularity is reduced by front-end electronics for the trigger, summing up to 60 channels into trigger towers. The resulting ∼7200 channels are transmitted to the trigger cavern with up to 70m long twisted pair cables. On the boundary of Calorimeter and Trigger responsibility the Receiver System applies analog operations on the signals,

[1] note that the typical signal is ∼5 ticks long, though, bearing the risk of signal superposition

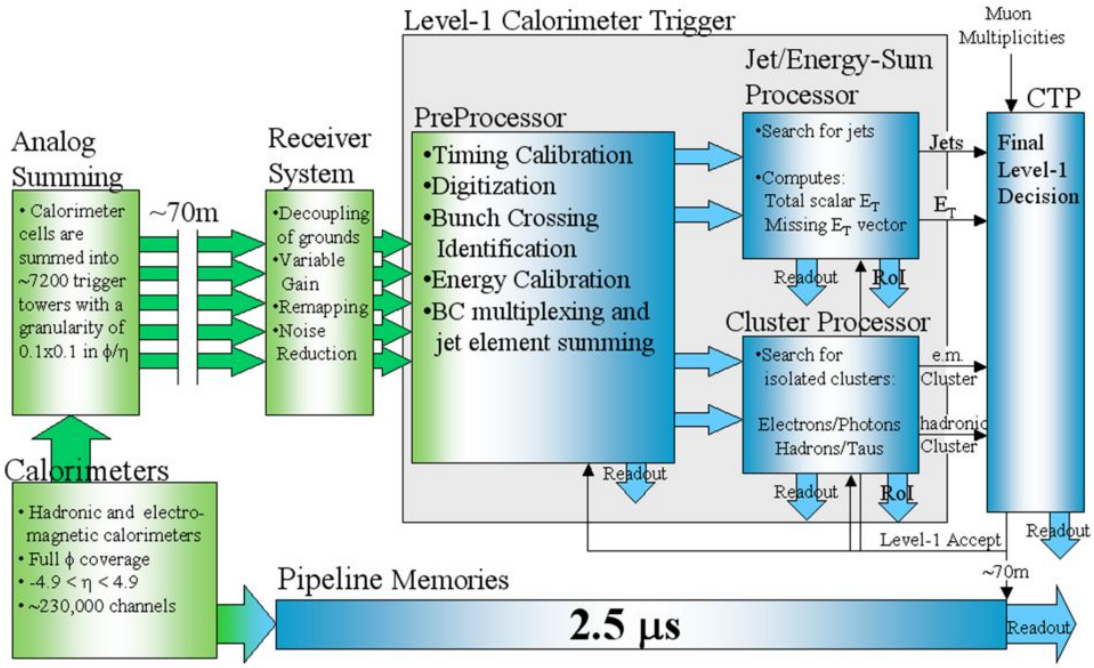

Figure 3.4: The Level-1 Calorimeter Trigger and its environment

before handing them to the L1 Calo Trigger Pre-Processor(PPr). There they are digitized, E_T is extracted and assigned to the correct bunchcrossing and energy and timing calibration is done. The results are send out via Low Voltage Differential Signalling(LVDS) to the two processors, the Cluster Processor(CP) and Jet/Energy-Sum Processor(JEP). The respective energy deposition patterns, electrons/photons and hadrons/taus for the CP and jets and global energy sums for the JEP, are searched for and the number of objects found passing certain thresholds is transmitted to the CTP. Intermediate data to document the decision making progress and the results are made available to the DAQ system at all levels.

The essential goals of the Level-1 trigger, to reach a decision every 25ns, accept no more than 1 of ∼500 events on average and take a maximum of 2μs for each decision, impose strict requirements on the L1 Calo Trigger and its subsystems. As a hardware trigger the parallel processing of multiple events is naturally achieved, the needed rejection power implies the need for high precision algorithms but the final decision is made at the CTP, so currently the most limiting of these requirements for the L1 Calo Trigger is the latency.

3.2.1 Analog input into the Level-1 Calorimeter Trigger

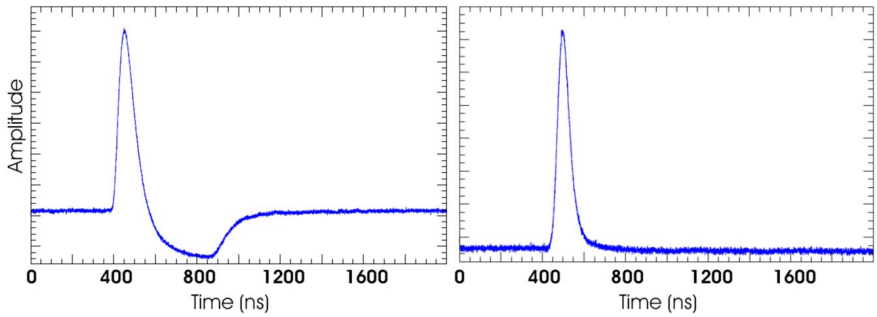

Figure 3.5: Typical LAr(left) and TileCal(right) pulse shape

As a sensible and predictable analog signal shape on the L1 Calo Trigger input side is essential for many of its tasks a short overview of the Receiver/Monitor system, the interface of the calorimeters and the trigger, is given despite it not being part of the trigger system. Its use was initially only foreseen for the Liquid Argon(LAr) calorimeters, but it is now clear that it will also be used for the Hadronic Tile Calorimeter(TileCal), where the L1 Calo Trigger collaboration is responsible for the line receivers.

The LAr calorimeter signals arrive in USA15, the cavern housing the Level-1 trigger electronics, on shielded twisted pair cables each carrying 16 differential signals. The TileCal signals arrive on different cables together with muon channels, but after a Patch Panel these are split off and cables arriving at the Receiver are identical to LAr ones. The Receiver system is built using 9-U VME boards with 4 analog signal cables on the input as well as the output. The functionality of the system, and also of a single Receiver board, can be divided into four sections[6]:

- Differential receiver section: A Transition Board mainly decouples front-end electronic and trigger grounds
- Variable Gain section: Four Variable Gain Amplifier(VGA) daughter-boards allow amplitude adjustments for each channel, to bring the signal level to E_T ratio to the required value at the receiver output
- Remapping section: The remapping board is primarily used to rearrange the order of the output signals to comply with L1 Calo Trigger needs[2]

[2]basically a block of $\eta \times \phi = 0.4 \times 0.4$ on each cable

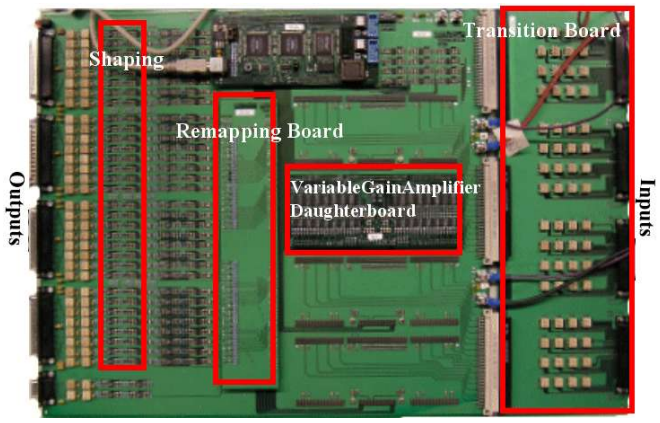

Figure 3.6: Picture of a Receiver Board

- Output section: a shaping stage with an RC-filter of $\tau = 5ns$, to suppress high frequency noise from the detector as well as the front-end electronics and the VGA daughterboards, and an output driver

3.2.2 Pre-Processor

The Level-1 Calorimeter Trigger Pre-Processor is the key interface between the analog world of calorimeter pulses and the digital world of trigger data and algorithms. At the input of the Pre-Processor ∼7200 analog trigger tower channels arrive from the receiver system, and the number of serial links transmitting digital LVDS data downstream to the processors is of the same order of magnitude. In between the signal is digitized after last analog adjustments, like f.e. phase adjustment and time calibration with the Phos4 chip[3], and the transversal energy E_T is extracted and assigned to the correct bunch crossing. The energy results are then fine calibrated using a lookup table before they are send towards the processors. For transmission to the Cluster Processor the channels are Bunch-crossing multiplexed(BC-mux) reducing the number of needed serial links by a factor of two, for the Jet/Energy-Sum Processor 4 channels are summed into a Jet-element, before the resulting data channels are serialized and sent out via LVDS.

The core achievement of the Pre-Processor is starting with an analog signal extending over several bunch-crossings(typically 4-5) and transmitting a single calibrated digital energy value in a single correct time slice to the processors. The central task of identifying the transverse energy deposition and the bunch-

[3] 4 channel delay generation ASIC with 1ns resolution, CERN Microelectronics Group

crossing in which the corresponding interaction occurred is called Bunch-Crossing Identification(BCID).

Building blocks of the Pre-Processor

The Pre-Processor is a very modular design. The basic building blocks holding most of its functionality are the MultiChipModules(MCM). Each of these is an independent system processing 4 trigger tower channels, and a single identical type is used for the full trigger space. To prepare the calorimeter signals for digitization, which among other things takes place on the MCM, interchangeable Analog Input Boards(AnIn) are used, one for each analog signal cable. A LVDS Cable Driver(LCD) board drives the long differential cables towards the processors and also takes care of signal fan out where needed. Four AnIns, 16

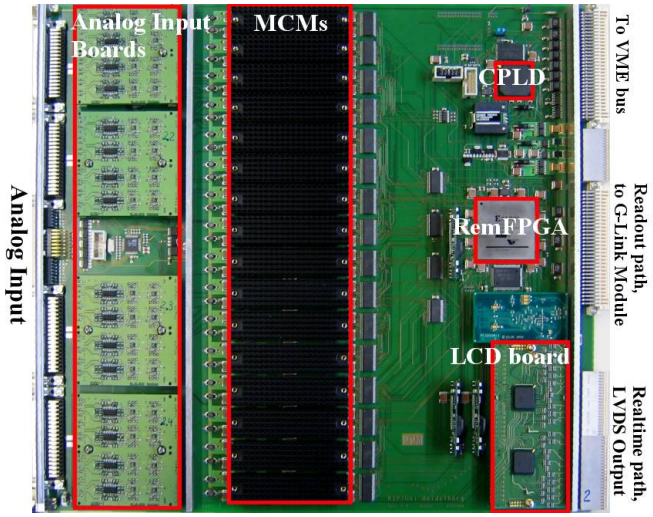

Figure 3.7: Prototype Pre-Processor Module

MCMs and one LCD board are mounted onto a 9-U VME printed circuit board resulting in the next, larger building block, the Pre-Processor Module(PPM). Logic for control and bus-handling for VME, all intra module communication and preparation of data for readout reside directly on the PPM, on a CPLD[4] and the Readout Merger FPGA[5](RemFPGA).

The complete Pre-Processor system consists of eight crates, containing 16 PPMs each. Additionally each crate has one crate controller CPU and one

[4]Complex Programmable Logic Device
[5]Field Programmable Gate Array

Timing-and-Control Module(TCM), as well as 16 rear-mounted G-Link[6] Transmitter Modules for the transmission of readout data to the DAQ system.

Analog Input Boards

The Analog Input Board is a printed circuit daughter board of the PPM performing several operations on 16 analog calorimeter channels. Signals on these channels are differential signals arriving from the Receiver System, with an amplitude of up to 3V which corresponds to 300GeV. The signal is converted to single-ended and the range from 0V to 2.5V(0 to 250GeV) is proportionally mapped onto the window of the FADCs[7] on the MCM, which is on average from 1.9V to 2.9V. DACs[8] on the AnIn boards allow to shift the signal's zero point in either direction for each channel, f.e. below the ADC window to suppress noise or up towards the middle of the window to make the negative undershoot following LAr pulses visible for the ADCs.

Moreover the AnIns provide a digital signal called external BCID, individually for all channels, by fanning out the analog signals to comparators with a programmable threshold. A 1 is written out when the signal passes the threshold, a 0 otherwise.

Multi-Chip Module

The four-channel Multi-Chip Module is a key component of the Pre-Processor, performing its most vital tasks:

- Rough timing calibration to bring all ∼7200 channels into the the same timeframe, to make up for differences in cable lengths and electronics latency in the signal path from the detector to the Pre-Processor
- Fine synchronization of the trigger channels, to sample all signals at their maximum
- Digitization of the signals
- Bunch-Crossing Identification, that is extracting the transverse energy from the digital pulse data and assigning the result to the correct bunch-crossing in which the particle responsible for the energy deposition originated
- Fine calibration of transverse Energy E_T

[6]G-Link is a transmission protocol
[7]Flash Analog-to-Digital Converter
[8]Digital-to-Analog Converters

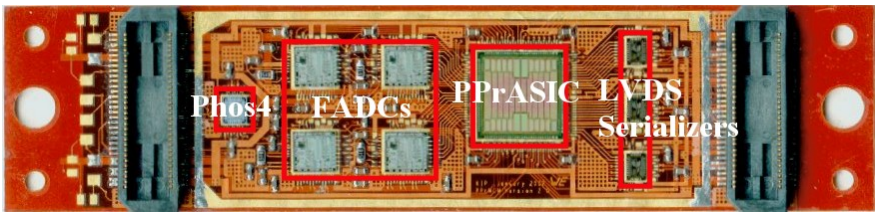

Figure 3.8: Picture of a MCM Prototype, before it is covered by a lid

- Preparation for transmission of the channels to the processors:
  - Summing of jet elements for the JEP
  - Bunch-Crossing Multiplexing(BC-muxing) of two CP channels onto one serializer channel to efficiently use the bandwidth and save cables
- Serialization and transmission of the real-time output using LVDS technology
- Readout tasks
  - Data playback capability to inject test data into the L1 Calo Trigger
  - Allow for pipelined readout of intermediate data and results
  - Histogramming and rate-metering to monitor the system performance

The Multi-Chip Module is a mixed signal design consisting of a small substrate residing on a copper heat sink with attached passive cooler, onto which a total of 9 chips are installed. Seven of them are commercial, four FADCs[9] digitizing the data using 10 bit precision and three single channel LVDS serializers[10], two for the channels to the CP and one for the JEP, each sending 10 bit data-words at 40MHz. One Phos4 chip is used for the fine synchronization of incoming signals, inserting delays of up to 25ns in 1ns steps. Moreover a RC filter is installed directly before the FADCs to suppress high frequency noise.

The Pre-Processor ASIC[11], a chip developed at the ASIC laboratory of the University of Heidelberg, is the core of the MCM conducting all digital processing on four trigger channels. At first a built in FIFO[12] buffer with a programmable length of up to 16 bunch-crossings brings all signals originating from one event into the same bunch-crossing. Then BCID is done with a combination of three

[9] Analog Devices 12-Bit 41 MSPS Monolithic A/D Converter, AD9042
[10] National Semiconductor 16-40 MHz 10 Bit Bus LVDS Serializer, DS92LV1021
[11] Application Specific Integrated Circuit
[12] First In First Out

methods[7]. For the first one a FIR filter[13] with a depth of five samples is used to improve the signal/noise ratio and is followed by a peak finder algorithm. It is highly efficient for most of the incoming signal range, from signals with amplitudes comparable to the noise level to close to the maximum digitization value which corresponds to 255 GeV.

As many calorimeter cells are summed into one trigger tower in the front-end electronics, saturation of the output amplitude can occur at several of the summing stages. For correct BCID of this cut off, flat-top signals another algorithm is used. It takes advantage of the fact that the correct incident bunch-crossing of these signals can be determined just from its rise, the energy result is set to the maximum of 255 GeV. Saturated signals are very important for the trigger, as they often strongly hint at interesting physics events.

The third mechanism is the external BCID provided by the AnIn boards and is mainly a fallback alternative and testing option for the other methods.

Two programmable thresholds divide the incoming signal level range into three regions and the BCID methods used can be specified for each region. The energy equivalent extracted from the signal using BCID is fine-calibrated in the Pre-Processor ASIC using a lookup table, which is also usable to f.e. suppress noise or subtract signal pedestals. All four channels of one ASIC are fanned out after the lookup table and summed into a single jet element for transmission to one LVDS serializer. Bunch-Crossing Multiplexing is applied to the main data path to result in the two cluster channels for transmission to the serializers designated for the CP. Hereby the nature of the analog calorimeter pulses and the BCID algorithms dictate that there is at least one empty bunch-crossing for that channel after each successful BCID. Taking advantage of this actualities allows this transmission of two cluster channels[14] on one link sending them in series.

Moreover histogramming, rate-metering and playback of test data is implemented using an internal memory in the PPrASIC and an interface for control and readout is provided.

Pre-Processor Module

The Pre-Processor Module is the carrier board for all other submodules, and is fitted to accommodate 4 AnIns, 16 MCMs and one LCD. It has three main output interfaces, to the crate controller CPU and TCM over the VMEbus[15], to

[13] finite impulse response filter

[14] as one ASIC provides only one jet element, BC-mux is not feasible for JEP channels; additionally due to the summing of four channels a jet channel can contain data in each bunch-crossing

[15] Versa-Module Euro, a crate backplane bus system

the DAQ system via rear-mounted G-Link cards and the real-time path towards the processors using parallel-pair cables carrying the LVDS signals. In addition some more interfaces and sub-modules are present for timing and control, f.e. a micro controller for slow control, a CAN[16]-bus interface and a TTC[17] decoder card.

The VME-bus handling and loading of the FPGAs on the PPM is done with a CPLD. The RemFPGA[18] is programmed to initialize, configure and control all submodules, as well as merge the data from all 16 MCMs in the readout path and send them to the G-Link Module.

LCD board

The LVDS cable driver board is a small printed circuit board which is plugged onto the PPM at the LVDS output. On board are two FPGAs and a large number of resistor and inductive component arrays. The purpose of the LCD board is to drive the signals over up to 15m of cable. The arrays act as precompensation for signal degradation on the cable, while the FPGAs are used as cable drivers, one for the cluster channels and one for the jet channels, and provide the fan out of signals required in ATLAS. Additionally rerouting of channels inside the classes is possible for non-standard setups in laboratory experiments or at the test beam.

3.2.3 Cluster Processor

The Cluster Processor(CP) receives digital serial data streams from the Pre-Processor, containing calibrated values of energy deposition in the calorimeters. Isolated clusters are searched, indicating either electrons/photons or hadrons/taus depending on the energy deposition in the hadronic calorimeter. The CP transmits the multiplicity of such clusters passing certain energy thresholds to the CTP, and makes Region-of-Interest and readout data available to the High Level Trigger and Data Acquisition system.

Functional view of the CP

The input data of the CP can be seen as two layers in η and ϕ, each layer consisting of an array of 50×64 E_T values[8], the layers corresponding to the electromagnetic and hadronic calorimeters. The CP searches for clusters using

[16]Control area network, used for the Detector Control System

[17]Timing, Trigger and Control; the system providing control, trigger and timing signals to the ATLAS sub-systems

[18]a Xilinx VirtexE 1.8V FPGA, XCV1000E

an algorithm based on a window of 4×4 values in each layer and the window is slid by single trigger towers in η and ϕ over the whole range. If the current position is a sharp local maximum a cluster has been identified and a RoI is defined. Each of these candidate trigger objects is compared to 16 sets of thresholds, and the number of objects passing each threshold has to be transmitted to the CTP.

CP implementation

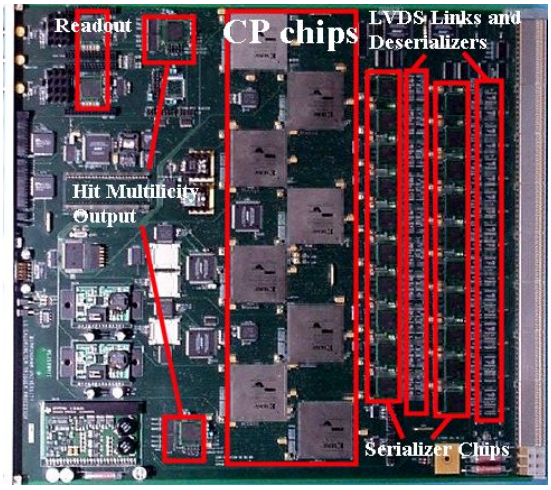

Figure 3.9: Prototype Cluster Processor Module[9]

The Cluster Processor consists of four crates with 14 Cluster Processor Modules(CPM) and two Common Merger Modules(CMM) each[19]. A single CPM processes data of a core area four trigger towers in η and one whole quadrant in ϕ, and overlap regions from the neighboring modules are shared on a custom backplane to allow the seamless use of the algorithm. The CMMs collect the multiplicities of clusters passing the thresholds from several CPMs and transmit them to the CTP.

Concerning a single CPM, data arriving from the PPM is received by the LVDS links and then deserialized and reserialized at a higher clock speed. The cluster finding and threshold testing is performed by eight CP chips[20], the algorithm implemented as firmware, before the data from all chips is collected again and delivered to a CMM.

[19] plus a crate controller CPU and a TCM as in all L1 Calo Trigger crates
[20] Xilinx Virtex-E FPGAs, XCV1600E

3.2.4 Jet/Energy-sum Processor

The Jet/Energy-sum Processor(JEP) receives reduced granularity data, sums of 2×2 trigger towers called jet elements, from the Pre-Processor to efficiently find jet signatures in the calorimeters. Furthermore it extracts total and missing transverse energy information. Multiplicities of jets passing thresholds are sent to the CTP, as well as the thresholds passed by the global energy sums. RoI information is provided to the DAQ system as well as readout to document the data processing.

JEP requirements and tasks

The JEP operates on an array of ∼30×32 jet element E_T values in each of the hadronic and electromagnetic calorimeters[8], received from the Pre-Processor. The granularity of a jet element is typically 0.2×0.2 in η/ϕ, and the corresponding hadronic and electromagnetic jet elements are summed into a single one upon reception. The jet algorithms identifies local energy clusters centered around a maximum using a sliding 2×2 element window similar to the CP. If a local maximum is found 2×2, 3×3 and 4×4 jet element energy sums centered on the maximum are calculated and compared to 8 sets of energy threshold/window size. The multiplicity of jets passing the threshold is sent towards the CTP for each set.

Moreover, the JEP performs two global summations of jet elements. The total transverse energy sum is a scalar sum over the full trigger space, though a programmable threshold for jet elements can be set to suppress background and noise. A total missing transverse energy sum is calculated by vector summing all jet elements, for which the vector components E_x and E_y are first computed locally using the ϕ coordinate.

JEP implementation

Due to the reduced granularity of jet elements compared to trigger towers, two crates each housing 16 Jet/Energy-sum Modules(JEM) are sufficient for the JEP. Each crate processes data from the whole η space(up to $|\eta| = 4.9$) and two ϕ quadrants. A single JEM has data from a core region of 4 elements in η and 8 in ϕ available and additionally overlap regions are shared over the backplane.

The JEM has evolved into a partly modular system, four input modules[21] receive the data from the Pre-Processor, deserialize the data and sum the hadronic and electromagnetic elements. One FPGA is responsible for the jet algorithm

[21] each having among other things one Xilinx Virtex-II 1.5V FPGA, XC2V1500

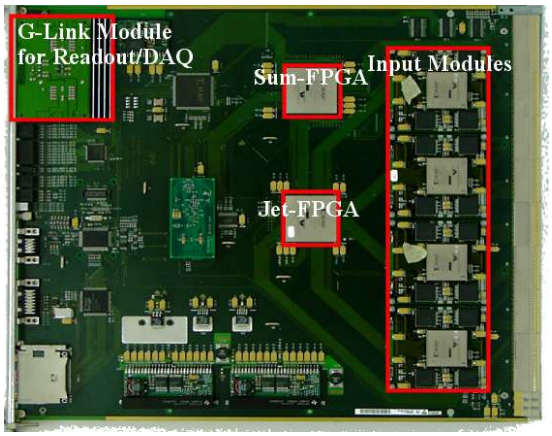

Figure 3.10: Prototype Jet/Energy-sum Module[10]

and one for the energy sum algorithms[22]. A G-Link module transmits data to the DAQ system while the jet candidates and energy sums passing thresholds are sent to CMMs in the crates.

[22]both are Xilinx Virtex-II 1.5V FPGAs, XC2V2000

Chapter 4

Test Strategy to evidence a working Pre-Processor System

As already described, the ATLAS Level-1 Calorimeter Trigger system has to process signals from several different calorimeter types with a total of ∼7200 trigger channels, and provide results allowing to lower the event rate for the High Level Trigger input by a factor of the order of 10^3. All this has to be done at an unprecedented bunch-crossing rate of 40MHz and a proton beam energy and luminosity resulting in an average of 23 inelastic proton-proton interactions per bunch-crossing, amounting to an input event rate of nearly one GHz. As the data of all $\sim 10^7$ detector channels has to be stored in on-detector Pipeline Memories while the Level-1 Trigger makes a decision, the practicability of this buffer system furthermore strictly dictates a maximum Level-1 trigger latency of 2.5 μs including the cabling from and to the detector.

4.1 Brief history of L1 Calorimeter Trigger tests

The feasibility of a trigger design with the above mentioned requirements is not given per se. The one briefly introduced in chapter 3, and in the ATLAS Level-1 Trigger Technical Design Report[8] in all detail, has evolved from a long series of test beam and laboratory runs using a small-scale version of the trigger during the calorimeter trigger demonstrator program. In this program several generations of hardware modules were used to test algorithms and technologies for the final trigger system, and ultimately prove the workability of the trigger concept.

The program successfully ended in 1998 when a system consisting of conceptual modules performing the tasks of the final system on a small scale had been used to prove the trigger concept, and the design for the L1 Calo Trigger was defined in the Technical Design Report.

Since that year the three subsystems of the L1 Calo Trigger[1] have been developed individually. Though each subsystem has been tested in a suitable laboratory environment or dedicated test bench while going through several iterations and design changes, no functional series of submodules in the real-time data path has been assembled for a long time. Concerning readout data, no full combined readout had been tested either.

In 2003 most modules had evolved into prototypes nearing suitability for production and plans for integration tests and a full slice test[2] became practicable. Furthermore a combined ATLAS Level-1 Trigger test beam run was scheduled for autumn 2004. This test beam period as well as the laboratory tests were the respective first opportunities since 1998, after huge individual development efforts and many design changes, and, with the perspective focusing on the Pre-Processor, are the subject of this thesis.

4.2 Collecting evidence for a working Pre-Processor System

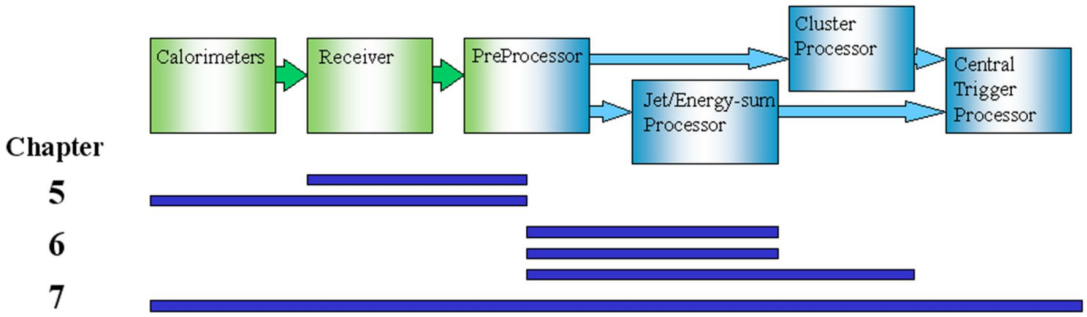

Figure 4.1: Diagram showing the range of the different tests and the chapters they are described in

The Level-1 Calorimeter Trigger Pre-Processor is not only a very modular system, but also close to a bottom-up design. Its essential tasks are performed by the PPrASIC, a custom designed chip to digitally process four trigger-tower channels. It is not only the fundamental building block of the Pre-Processor system but consequently was also one of the first components to be finalized. The Multi-Chip Modules carrying the PPrASIC and supplementary chips were

[1] Pre-Processor, Cluster Processor and Jet/Energy-Sum Processor as described in chapter 3
[2] test of the full Level-1 calorimeter trigger system in a laboratory environment

the next component available in a final state. Though real production prototypes only began to become available during the time of writing, prototypes identical in functionality and design but produced using other production processes have seen extensive testing. The Analog Input boards and the PPrASIC have gone through one iteration during internal tests, but only minor issues needed to be fixed.

All of the above components have been tested using a dedicated test bench, the Pre-Processor Test System, and were found to perform correctly and inside their specifications as far as this can be determined by standalone tests. That of course is no substitute for tests using the final carrier board and/or combined with the other L1 Calo Trigger subsystems, nevertheless the verification of the functionality in internal Pre-Processor tests was a great success and essential groundwork for integration into the full system. This integration, also aiming at a combined test beam, was foreseen and done in three functional blocks(although they do not correspond to time periods, but were partly done in parallel).

The Pre-Processor as interface of the trigger to the calorimeters

One vital role played by the Pre-Processor in the ATLAS experiment will be the interface between the analog signals and electronics of front-end modules and calorimeters and the digital data processing of the trigger. In order to prevent issues of the resulting two interfaces of the PPr from negatively impacting the testing and debugging of the respective other one, it has been a goal of the PPr group to sort out both separately at first.

Thus one of the blocks of integration of the PPr into its full environment was dedicated to the analog signal chain upstream of it. The first tests were done together with the system directly preceding the PPr, the Receiver system, which is the interface of the calorimeters to the Pre-Processor. Successfully completing these the signal chain was then extended up to the calorimeters at the ATLAS H8 test beam at CERN, making good use of a test beam period prior to the combined one of the Level-1 Calorimeter Trigger.

Setups, tests and results of the analog interface of the PPr are presented in chapter 5.

Testing the functionality of the Level-1 Calorimeter Trigger processing chain

The next group of tests includes experiments inside the Level-1 Calorimeter Trigger. Solely focusing on digital data transmission and processing, these tests were done in laboratories mainly using direct injection of digital test data. This work was done in parallel to the integration of the PPr into the analog signal

chain.

At first combined setups of the PPr and the JEP were tested, due to logistical reasons as these could be done in Mainz. After that integration of the PPr and CP, and finally an attempt of a full system test, was done at the Rutherford Appleton Laboratory in England.

Full account on the Mainz tests and an overview of the tests in England are given in chapter 6.

Verification and tests of the full L1 Calo Trigger at the test beam

The final step to prove a correctly functioning system was a combined test beam of the full ATLAS Level-1 Trigger and the calorimeters, with timing and control of the systems under realistic conditions. Contrary to the other two phases, where only either the analog or digital interface of the Pre-Processor was examined, it would now have to fulfill its role as connector between the analog signals and systems and the digital processing in the trigger like in ATLAS. Ideally the approach would have been to take the systems to the test beam when the analog signal path from the detector to the PPr as well as the digital L1 Calo Trigger system are fully and individually debugged and tested in a controlled environment. Time constraints forced the integration of the L1 Calo Trigger systems into the combined test beam run before a full digital system test in a lab had been successful, though.

The combined test beam period with a duration of about six weeks was still in progress during the time of writing. Its proceedings and first results are presented in chapter 7.

As an addition to the above strategy, an attempt was made to do as much work as possible using the Pre-Processor Test System to lower the pressure and save time for testing with the PPM, as it was the last L1 Calo Trigger module to be available.

In summary the testing strategy proved to be fruitful, as results in chapters 5 thru to 7 will show, though strict timing constraints resulting from the fixed test beam schedule and the development work needed in parallel to the testing did not allow to fully bring it to bear.

4.3 Dedicated test systems

Not all systems and components used during testing will be part of ATLAS, or are set up as in ATLAS. As these are thus not described in chapters 2 or 3 a

short introduction will follow for test environments which are relevant for more than one setup of the following chapters.

4.3.1 The ATLAS H8 Test Beam at CERN

The ATLAS H8 Test Beam is located at the Super Proton Synchrotron(SPS) North Area(Prevessin, France) of the CERN, where to the SPS beam is extracted for various test beams. The H8 test beam setup uses barrel modules and components of ATLAS detectors to simulate a small sector of the ATLAS detector barrel region. This section will shortly introduce the setup in place during the year 2004. Some parts of the setup directly correspond to ATLAS, but are included here to provide more details than in section 2.2 starting on page 4.

Beam characteristics

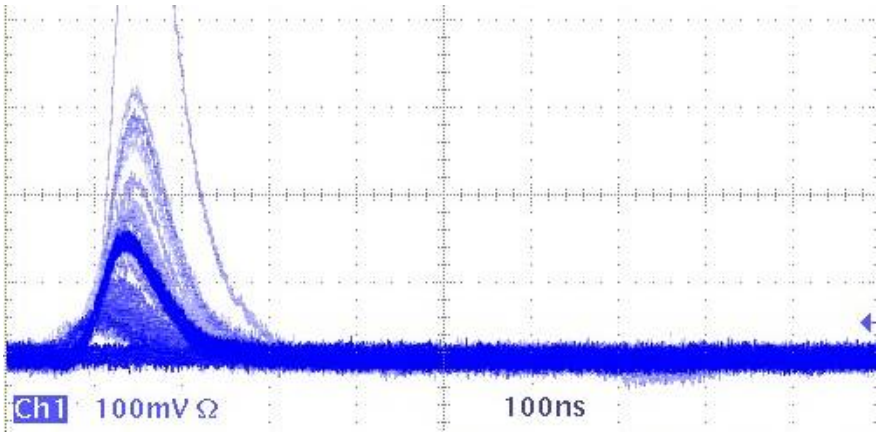

Figure 4.2: Oscilloscope picture of a pion beam spill in a TileCal Trigger Tower

The SPS beam consisted of protons with an energy of typically 400 GeV(with a maximum of 450 GeV). In normal operation the SPS did not supply a beam structured comparably to the LHCs tight bunches in 25ns intervals, but instead long spills of ∼4.8s in lenght, one spill occuring every ∼16.8s. But as the SPS will be part of the accelerator chain for the LHC, operation in a mode with 25ns timed bunches was tested for short periods.

For the H8 test beam the SPS proton beam was mainly shot at a target, where a beam of secondary particles was created. With the H8 beam optics a combination of particle type and energy could be selected for use, typically pions or electrons with energies up to 250 GeV. A tertiary beam of low energy particles(2-10 GeV) and the attenuated primary proton beam also were available.

Detector Setup

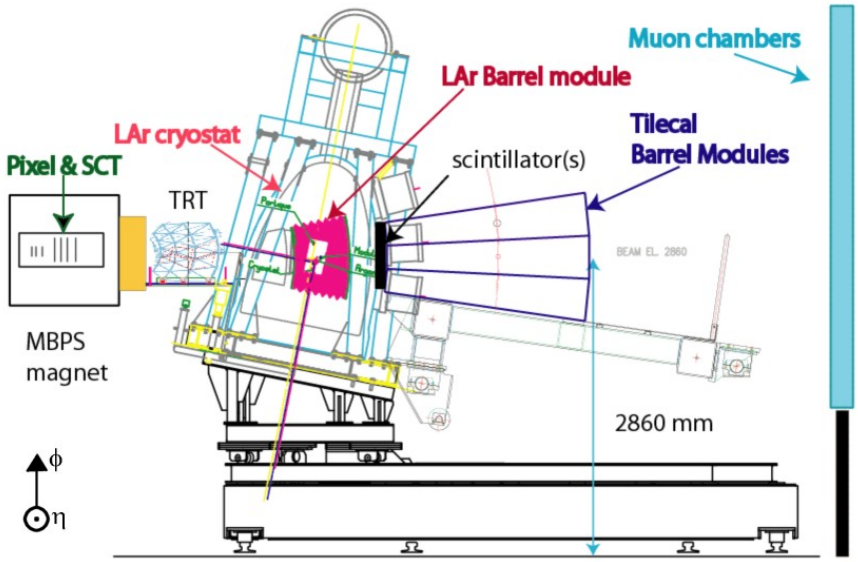

Figure 4.3: Diagram of the placement of detector modules at the H8 test beam[11]

The concept of the H8 test beam setup was to simulate a section of the ATLAS barrel, with modules from all detector types being positioned in series comparable to the full ATLAS detector. The beam line is considered to go through a virtual point of interaction and the η/ϕ-planes of detector modules were positioned in a right angle to it. The final beam position in the detectors depended on a set of magnets at the virtual point of interaction, and could be moved in both the η and the ϕ direction.

Concerning the calorimeters, the only items of interest in this context, one LAr electromagnetic barrel module and three hadronic TileCal barrel modules were installed. The LAr module covered an area of 0.4 in ϕ and 0.0 to 1.5 in η, while the TileCal modules covered a total of 0.3 in ϕ and -1.0 to +1.0 in η. All modules shared the phi direction and the $\eta = 0$ plane, meaning only one half of the TileCal Modules had the LAr module in front of it. Technically the TileCal modules had been installed the wrong way round in respect to the LAr module, resulting in η increasing in opposing directions. As the TileCal Modules are fully symmetric in η and the halves of the modules not covered by the LAr module did not receive any beam, though, this issue will be neglected in the following and all η values are to be considered absolute values, shared by all modules.

In respect to ϕ both calorimeters were centered around the beamline. As a result the LAr module could be considered to be shifted down by 0.2 in ϕ

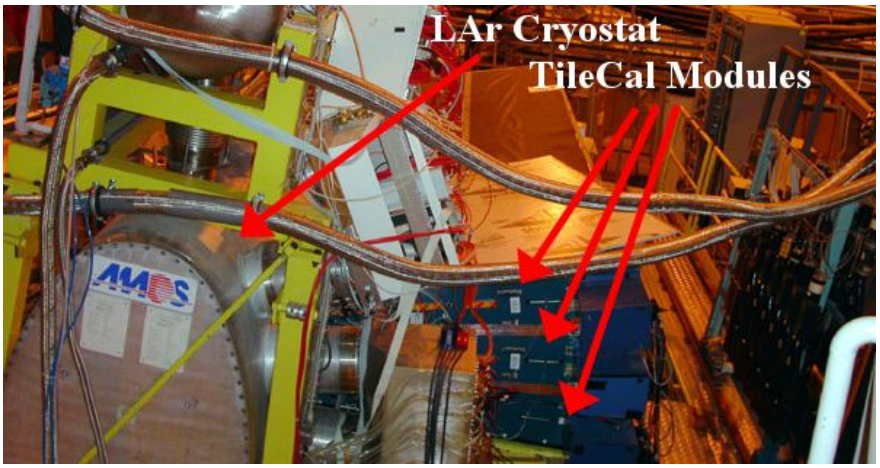

Figure 4.4: Photograph of the calorimetry at the test beam

comparing it to ATLAS, and the TileCal by 0.15. In other words, the LAr calorimeter covered $-0.2 < \phi < +0.2$ and the TileCal $-0.15 < \phi < +0.15$.

A calibration system was in place for the LAr calorimeter as well as the TileCal, allowing to directly inject precise amounts of energy to obtain pulses for calibration work, which are very similar to pulses resulting from energy deposition of beam particles. These systems could also be used to provide signals for the L1 Calo Trigger.

Trigger towers and cables

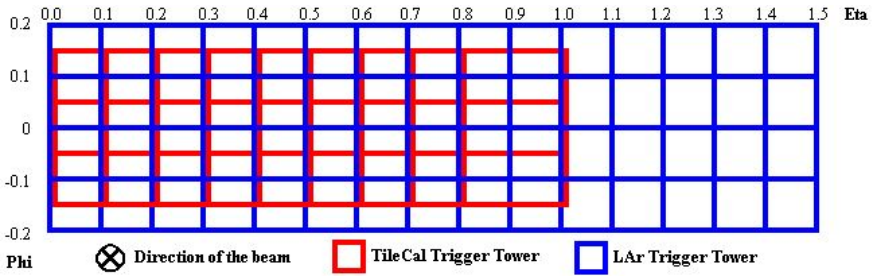

Figure 4.5: Simple diagram of Trigger Towers at the test beam, in η/ϕ-space

The front-end electronics summing calorimeter cells into trigger towers, Tower Builder Boards(TBB) for LAr and 3-in-1 boards for the TileCal, were set up and cabled like for ATLAS. This resulted in the typical trigger tower size of 0.1×0.1 in

$\eta \times \phi$[3]. The downward shift of the calorimeters in ϕ by different values to center them around the beam had an important consequence here as the electromagnetic and hadronic trigger towers overlapped by half, making f.e. summing of total energy deposition in one jet element in the JEM less practical (see figure 4.5).

Three cables had been laid from the detector to the trigger control room for each calorimeter type, the TileCal cables having a lenght of 60m, the LAr ones 70m. As the TileCal signals went trough a patch panel and another 10m of cable before arriving at the receiver system, the lenght of all cables from the calorimeters to the trigger was roughly equal.

Each TileCal cable carried signals from one η half of one module, and so from an area one ϕ bin high and 9 trigger towers wide from $0 < \eta < 1$. Likewise each LAr cable had 15 trigger towers channels, from one ϕ bin and all η values of the module, $0 < \eta < 1.5$. This corresponds to the setup of ATLAS.

Concluding, all trigger towers signals of the TileCal at the test beam arrived in the trigger control room, whereas the LAr calorimeter has four ϕ bins of which only three can be selected due to the limited number of cables. Furthermore two TBB boards are needed to cover the LAr ϕ range but only one was installed most of the time, only allowing to either access the lower or higher ϕ half of the module.

Detailed information about trigger tower mapping and cabling at the test beam or in ATLAS can be found elsewhere([12], [13]).

Timing and trigger

Timing and the transmission of L1 Accept signals was shared by all detector and LVL1 trigger components. Generation and distribution of these was done by the CTP group.

The clock during normal SPS operation was a TTC generated 40 MHz clock, not linked to the beam structure. Most importantly for the Pre-Processor this meant that it was impossible to calibrate the timing between the arrival of a signal and the clock, the signals freely floated in respect to the digitization points. This did hence not allow to optimize BCID coefficients or to fine calibrate resulting energies.

During 25ns mode operation of the SPS, the clock was provided by the SPS and signals arrived in a fixed relation to the clock. Moreover a clock in sync with the calibration signals generated by the calibration system could be provided in all modes.

The L1 Accept signals was generated by two methods. The first was a mock-up CTP basically consisting of a simple beam trigger, originating from scintillat-

[3]with the exception of the outermost TileCal towers, in ATLAS an overlap region with the TileCal Extended Barrel, which span from η 0.8 to 1.0

ing counters in the beamline and delayed by the expected Level-1 latency. The second method, planned for the end of the full Level-1 Trigger run, was a real CTP prototype supplied with information from the Level-1 trigger subsystems.

4.3.2 The Pre-Processor Test System

The Pre-Processor Test Environment is primarily designed as a test bench for components of the Pre-Processor. It was used for countless experiments to validate the functionality of prototypes of AnIn boards and MCMs and will play a vital role in production tests of the latter. The system consists of a custom VME crate and the Pre-Processor Test Board. It simulates the complete environment of a PPM: analog input from the calorimeters, control with a crate controller CPU, reception of real time data by the CP or JEP and readout. It is thus perfectly suited for laboratory experiments, substituting some actual modules for parts of the test system in the case of integration tests.

Only a brief overview over the system will be given, a detailed description can be found elsewhere[14].

Analog Signal Source

The signal source for the test system is an off-the-shelf commercial graphics card. It is used to replay calorimeter pulses recorded at the test beam or arbitrary test pulses. The card has three analog outputs(the color channels), and two digital synchronization signal outputs[4] and test signals can be generated by displaying a screen. The three 8bit color values of each pixel are given out as a voltage from 0 to 700mV and with the refresh rate and screen size used in all tests, each pixel is send for 5ns. Pulses can thus be generated with a time resolution of 5ns and an 8bit resolution amplitude between 0 and 700mV, individually for all three independent channels. As the rise time of a generated pulse is not zero, which would result in the creation of step functions, but fully sufficient for calorimeter pulses the output is a nice representation of real signals.

One of the digital synchronization signals provided is also used, and supplied to the test board to be able to synchronize its clock with the analog signals.

Concluding, the analog signal source is a good replacement for a three channel function generator, with the advantage that is easily and most foremost quickly programmable, allowing for fast automated signal changing during tests.

[4]actually twice that numbers, but the other outputs are used for a computer monitor

The Pre-Processor Test Board

The Pre-Processor Test Board is a small printed-circuit board, emulating many functions of a PPM. It acts as carrier board for a single Analog Input board and one MCM, both final components of the trigger system and described in section 3.2.2 on page 23. With those two modules the test board has access to all vital functions of the Pre-Processor for up to four channels.

As single ended analog signals arrive from the signal source with a maximum amplitude of 700mV, the input stage of the test board converts them to differential signals with an amplitude of up to 2.5V, corresponding to the input in ATLAS. The digital sync signal is received by a Phase Locked Loop(PLL) which derives, together with a CPLD as frequency scaler, a 40MHz clock for the MCM[5].

The VME Crate System

A custom VME crate with three 6U custom printed-circuit boards and a crate controller based on a standard PC motherboard forms the last component of the test system. From a functional point of view the crate system performs three tasks:

- Control of the whole test system, including initializing of the MCM and AnIn and controlling the signal source
- Reception of the real-time LVDS data channels from the MCM, making them available to readout
- Accessing data from the readout path of the MCM

While these functions resemble the ATLAS setup closely enough to thoroughly test the Pre-Processor components there are differences. Firstly control of the system is based on a standalone software not connected to the Online Software of ATLAS DAQ. While the MCM and AnIn are addressed like in ATLAS, all higher level communication is done differently to better suit the circumstances. This also applies to the readout data path where raw data is collected instead of merging readout of several MCMs and encoding it. The real-time path data is additionally impeded as it is first written onto a memory residing inside an FPGA on one of the 6U VME boards and then read out over the VMEbus. As this readout is too slow, the LVDS data can't be read continuously but only in chunks(the size of the memory) with large gaps in between. Also readout and real-time data cant be accessed in parallel as they both need to be buffered in the same memory.

[5] a quartz clock is used in absence of a sync signal

All in all the Pre-Processor test system is a viable test bench for production tests, and can be used for wafer tests of PPrASIC chips as well as tests of the assembled MCM. It is also an option in a lab environment to substitute for the systems interfacing with the Pre-Processor, but can not replace tests including all final Pre-Processor components. That being said, with the addition of a single-ended to differential converter board the analog signal source is very useful to test PPMs or supply analog data for integration tests in a lab.

Chapter 5

Testing the analog signal chain up to the Pre-Processor

While the final goal of the Level-1 Calorimeter Trigger integration tests is a run with the full system including the upstream systems up to the detector, the first priority of the Pre-Processor group was to isolate the two environments of the Pre-Processor, the analog side of calorimeter signals and the digital processing of the trigger, for initial experiments. In this way the analog signal chain and the cooperation of the digital parts of the trigger can be debugged on their own under simpler and more transparent conditions.

Concerning the analog side, the Pre-Processor was tested together with its direct predecessor in the signal path at first, the Receiver System, before the setup was expanded up to the calorimeters at the test beam.

5.1 Receiver/Pre-Processor tests

The integration of the L1 Calo Trigger Pre-Processor and the Receiver System in Heidelberg was a joint achievement together with the Receiver group from the University of Pittsburgh during February 2004. The motivation, apart from the incentive to examine the Pre-Processor's analog input side, was to make certain that the signals provided by the receiver system comply to Pre-Processor expectations and requirements. Though the BCID algorithms would allow for some adaption to different signal shapes, they were designed aiming at maximum efficiency with certain pulse shapes. As the algorithms are, apart from parameters, fixed in the PPrASIC it is thus highly desirably to make sure that the whole analog chain, with the receiver as last stage, supplies sensible signals resulting in high BCID efficiency. The tests were done in the light of the oncoming Production Readiness Review(PRR) of the Receiver System to validate its design

before production.

The testing was done with the Pre-Processor Test System and the results were first presented in a short note which was prepared for the Receiver PRR[15].

5.1.1 Test setup

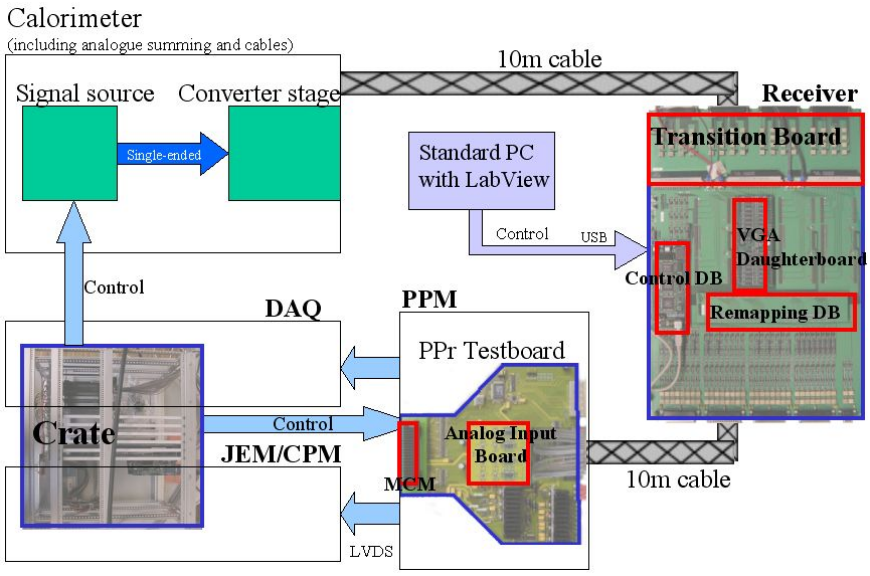

Figure 5.1: Test Setup, the outlined boxes represent ATLAS systems substituted by test system components

Signal source

The signal source used is the graphics card that is part of the Pre-Processor test system. It provides three single-ended analog channels programmable with a resolution of 5ns in time and 8bit in amplitude. The conversion to a differential signal is normally done on the test board, but for this test an external solution able to drive the twisted pair analog signal cables[1] was needed. A small amplifying stage was used, also fanning the signals out to 4 channels and allowing to individually supply each signal to one of the 16 channels of the cable.

Pulses from the Hadronic Endcap Calorimeter(HEC)[2] recorded at a prior ATLAS test beam[16] were replayed for the tests. The characteristic negative

[1] prototypes of the cables used in ATLAS

[2] a liquid Argon technology sampling calorimeter

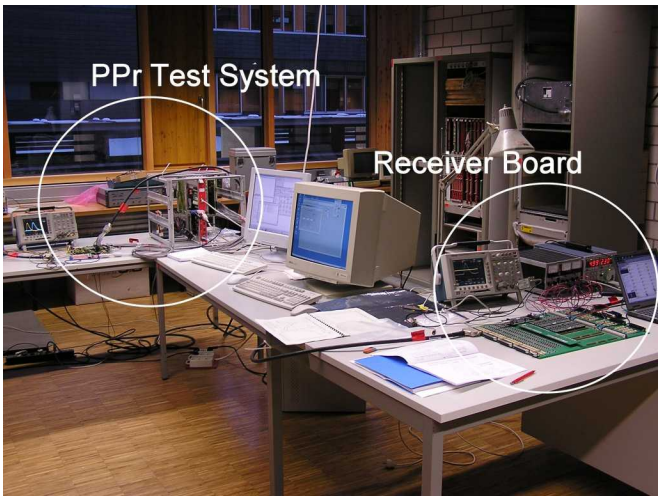

Figure 5.2: Photograph of the test setup

undershoot of these pulses, with a length of up to 500ns, was cut off during replay, to bunch signals closer together and to use the full amplitude resolution for the positive main part of the signal. Except for the risk of superposition the undershoot plays no role for BCID in ATLAS. Some tests needed to be done using pulses recorded using the HEC calibration system, in contrast to energy deposition by particles, as the range of recorded particles was not sufficient.

Receiver/Monitor Station

One Receiver Board was set up in Heidelberg for standalone tests, that is including a USB controller daughterboard while in ATLAS control will be handled by one specific board per crate. The Receiver Board was equipped with one Transition Board, a single Variable Gain Amplifier(VGA) daughterboard, as a maximum of only four channels carried signals in the setup, and one Remapping Board. The Remapping Board used is coincidentally one designed for a HEC region in ATLAS, but was chosen because it directly and straightforwardly maps inputs onto the outputs, which is best suited for this setup.

The output stage of the Receiver Board initially tested had a low pass filter with a time constant τ of 15ns as the decision to change τ to 5ns, as the system is described in section 3.2.1, was a consequence of the tests.

Pre-Processor Test System

The Pre-Processor Test System was largely unchanged from a standard setup for standalone MCM tests. As indicated above, the analog signal path was opened directly after the signal source, and a small converter stage and the Receiver Board inserted. The output of the Receiver was supplied directly to the AnIn board. Otherwise the closed circuit of control and readout by the VME Crate System stayed intact. The crate system played the roles of the processors receiving the LVDS output of the Pre-Processor, the calorimeters and a simplified readout system.

Types of measurements

The tests focusing on the shape of analog signals, all measurements presented in the following were done with an oscilloscope. Digital data, namely BCID results, were looked at to confirm conclusions derived from pulse shapes, but no systematic long term tests were done. Though correct BCID results will be the only thing of importance in the ATLAS trigger, the final result of the tests the receiver system leaves the analog pulse shapes unchanged and thus all prior experiments which validated the BCID mechanism in absence of a Receiver Board stay valid.

A sufficiently fast digital oscilloscope was used, measuring the signals with a differential probe at the inputs of the Receiver Board and the AnIn board. A 20MHz bandwidth low pass filter was applied to emulate the filter residing on the MCMs directly in front of the FADCs.

5.1.2 Tests and results

Connectivity of the systems did not pose a problem at any time. Furthermore operation of the system went flawlessly, the needed calibration to replay pulses with their respectively correct amplitude in the system, including the amplifying stage and the receiver, being the only time consuming factor.

The first tests were done using signals with a standard shape, corresponding to a particle energy deposition of roughly 50 to 150 GeV. As saturation of the signal level can occur in several of the analog summing stages of the ATLAS detector in case of a energy deposition corresponding to more than 300GeV in one trigger tower, tests were also done with the resulting flat-top signal shapes. As no recorded beam pulses had high enough energies for saturation of a trigger tower, pulses recorded using the calorimeter calibration system were used. These had been created by direct charge injection into the calorimeter and closely resemble real pulses.

Lastly the linearity of the VGA voltage input range was examined. The system was believed to comply with the requirements of input from LAr calorimeters, but as the decision had been made to also use the receiver system for the TileCal calorimeter channels it needed testing with the higher maximum amplitude of the TileCal front-end electronics.

Tests using non-saturated pulses

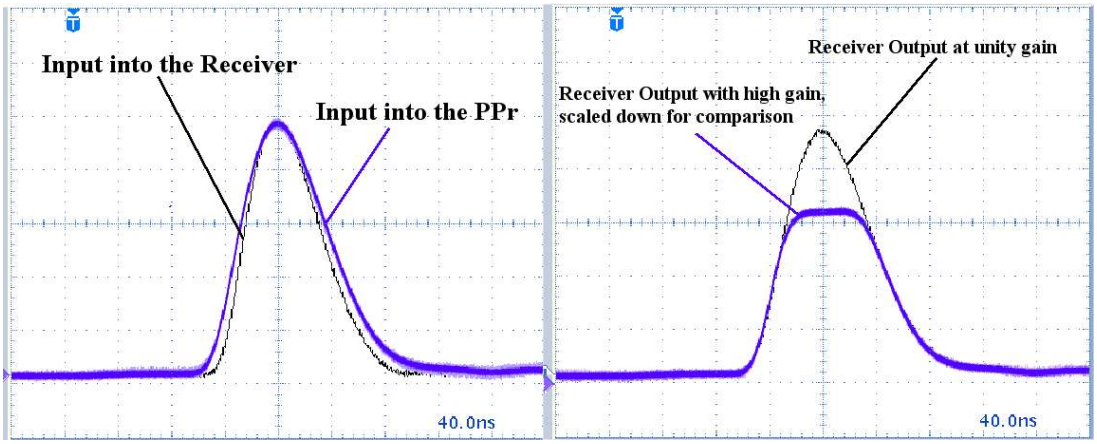

Figure 5.3: Scope pictures showing the effect of the receiver on the pulse shape(left) and clean clipping of the signal by the receiver(right)

The first tests were done using signals with no more than 2.1V amplitude at the receiver input, which is roughly the maximum expected LAr signal amplitude after the 70m of cables into the trigger cavern. Signals with the normal LAr signal shape, not cut off or saturated during analog summing of the trigger tower, were replayed without the long negative undershoot of the signals, being not relevant for these tests.

As can be seen on figure 5.3 on the left the pulses were expectedly broadened a bit by the low pass filter on the receiver, but otherwise the signal shape was conserved. In addition a pre-prototype remapping board with summing circuitry was tested, and found fulfilling its purpose.

The same test signals were also used to examine clipping of the signal in the receiver. Resulting from high gain settings on a VGA daughterboard or summing on the remapping board the output of the receiver could exceed the maximum input range of the Pre-Processor, set at 3V. The output stage of the receiver is required to clip the signal at 3V in these cases. The picture on the right of figure

5.3 demonstrates that this clipping is done nicely without distorting the pulse shape.

Tests using saturated pulses

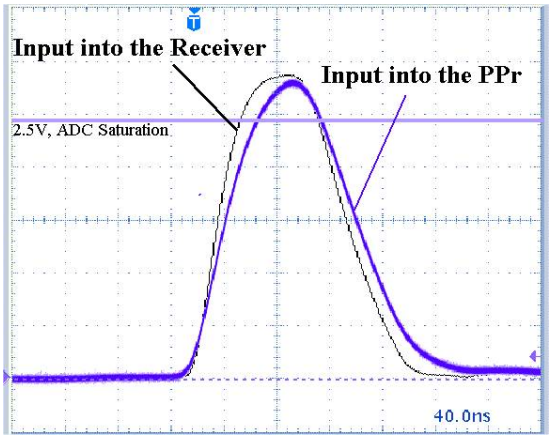

Figure 5.4: Saturated calibration pulse

So called saturated pulses result from saturation of operational amplifier outputs during the summing of calorimeter cells into trigger towers. This occurs in the LAr front-end electronics when objects deposit energy corresponding to an E_T of more than 300 GeV in one trigger tower. As trigger objects with energies in that range strongly hint at an interesting physics event, it is crucial for the trigger to get a correct BCID. The BCID algorithm used in the Pre-Processor for these pulses determines the bunch-crossing in which the object originated from the rise of the saturated signal, as the peak is clipped off. No information can be gained from the flat top and taking the falling edge into consideration would lead to a significant increase of latency due to the lenght of the signals.

The tests showed that the shaping stage at the receiver output, having a time constant τ of 15ns, slowed the leading edge of saturated signals significantly down(see figure 5.4).

To examine the behavior of the VGA daughterboard with saturated pulses the RC filter of the output stage had been taken out for one channel. The resulting input to the Pre-Processor, shown on figure 5.5[3], made oscillations of the operational amplifiers visible. The filter evened these out again, but the treatment of the signal shape was nonetheless not optimal.

[3]The replayed pulse had been scaled up a bit resulting in a steeper rise to study the effect

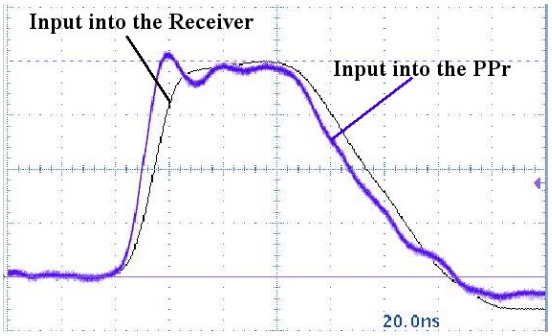

Figure 5.5: Scope shot with Receiver RC filter taken out

Testing the linearity of the VGA input range

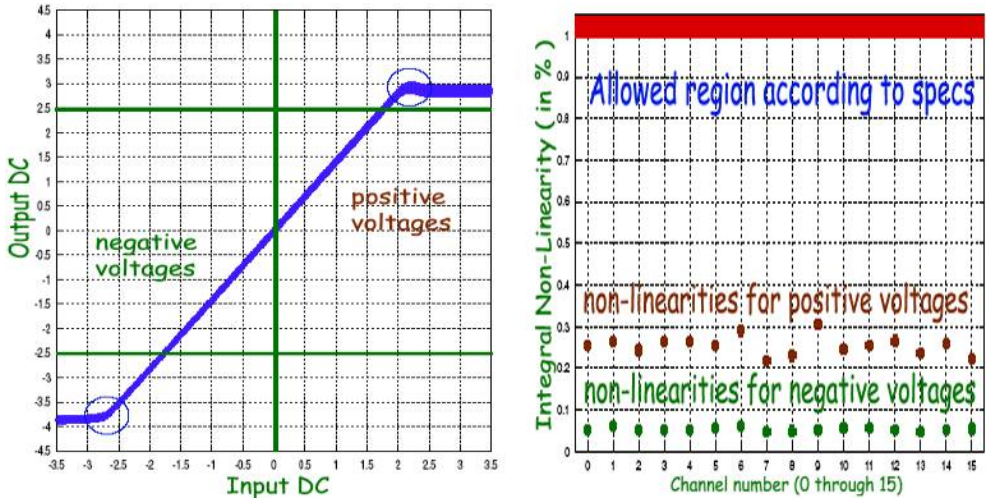

Figure 5.6: Input range and integral nonlinearities of a VGA daughterboard, measured with fixed gain[17]

Extensive tests have been done by the Pittsburgh group regarding the acceptable input range and integral nonlinearities of the VGA daughterboards[17]. Their voltage input/output ratio is highly linear from -2.6V to +2.1V(see figure 5.6), beyond these points the output saturates. These values are sufficient for the LAr calorimeters when 70m of cables are used to connect the receivers. As there is a possibility for the use of shorter cables(resulting in higher amplitudes) and most importantly considering the use of the receiver system for the TileCal calorimeters where the saturation level in the front-end electronics is higher, the

VGA input range was also tested in Heidelberg. Furthermore saturated signals had not been available for the tests in Pittsburgh, non-saturated ones had been used for the whole voltage range.

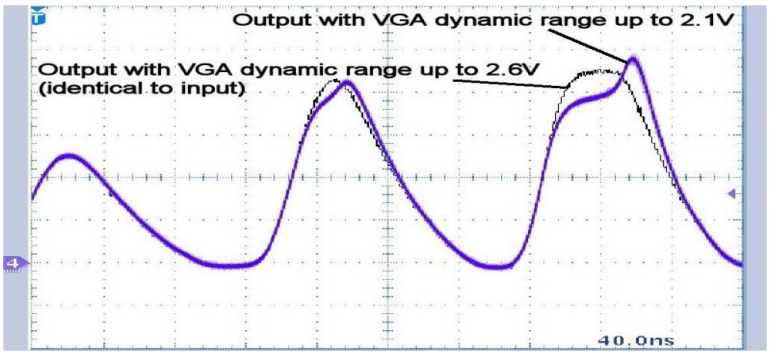

Figure 5.7: Input to the Pre-Processor with a receiver input amplitude up to 2.2V, with positive(blue curve) and negative(black curve) input

The test signal used was an artificial ramp of HEC pulses with undershoot cut off and closely bunched together, rising in corresponding energy up to saturation. The tests were done with a shaping time constant of 5ns on the receiver(see section 5.1.3 on page 52), and using positive and negative pulses for comparison. Only positive pulses will occur in ATLAS.

As shown on figure 5.7, significant distortions of the pulse shape are visible already slightly above saturation level of the VGA daughterboards.

5.1.3 Conclusions and consequences

The Receiver System was found to generally perform well inside its specifications using non-saturated pulses as input, and standalone test results from Pittsburgh could be confirmed. When pulses saturated in the front-end electronics were used as input, which was done in Heidelberg for the first time, some issues came up demanding changes to the Receiver Boards. Furthermore with the planned use of of the system for the TileCal calorimeters specifications regarding the voltage input range had to be revisited and hardware changes were needed.

Conclusions of the saturated pulse tests

Though the BCID algorithms are fixed inside the PPrASIC, parameter sets allow to adjust to pulse shapes different from expectations of the time they were designed. The influence of the receiver system on saturated pulses, significantly

slowing the initial rise and introducing intermediate distortions during signal processing, could probably be coped with by the Pre-Processor[4]. But the possibility to adjust the BCID parameters can be seen as a contingency reserve for further unexpected effects in the analog signal path, and thus all known issues like the above should be solved if possible instead of cutting into this reserve.

It was therefore decided to change the time constant τ of the receiver filter stage from 15ns to 5ns. With this setup, the pulse shape is unchanged by the receiver which is considered to be ideal for BCID. Furthermore back termination was added to the long lines from the VGA daughterboards to the remapping board, which solved the op-amp problems found on the VGA.

Consequences of the changes to the Receiver shaping stage

The shaping stage is implemented on the receiver to suppress noise, mainly high frequency noise resulting from the operational amplifiers in the front-end electronics and the VGA daughterboards. As such the time constant of 15ns was chosen based on noise estimates in receiver design reports. The change to 5ns made it necessary to revisit these.

It was found[18] that the original estimates did not include the effects of the cables from the detector and the low pass filter on the PPr MCM. The noise reduction of 70m of cable is comparable to a shaping stage with a time constant of 15ns, while the MCM filter has a τ of roughly 7ns.

	Design Report	5ns shaping(+cable+MCM)
Upstream op-amps	73 MeV	52 MeV
VGA noise	50 MeV	55 MeV
Total electronics noise	88 MeV	75 MeV

Table 5.1: Comparison of noise estimates

As shown on the table, the total electronics noise is expected to be below the estimate from the receiver design report, despite the slight increase of VGA noise which is naturally not filtered by the 70m cable. Concerning calorimeter noise the situation is also improved, as the cables alone make the shaping stage on the receiver dispensable. The new parameters for the receiver board result in sufficient noise reduction and thus the changes are feasible.

With the pulse shape effectively unchanged by the receiver, it is much closer to Pre-Processor expectations and correct BCID is easily achieved with full effi-

[4]No high statistics BCID efficiency measurements were made

ciency. Furthermore BCID algorithm parameters remain as a valid contingency reserve for possible future issues.

VGA input voltage range adjustments

The conclusion to the tests concerning the VGA input voltage range was that significant distortions appear uncomfortably close to the maximum input voltage of LAr signals after 70m of cables, leaving no contigency for shorter ones, and that the linear region is not sufficient for use with TileCal signals.

Figure 5.6 on page 51 shows that not only the VGA input range is linear up to a higher absolute value on the negative voltage side, but also integral non-linearities for the negative region are smaller. In consequence of the Heidelberg tests the design was hence changed to run the Variable Gain Amplifiers in inverted mode. Moreover a placeholder for a voltage divider was introduced on the daughterboards, to be able to increase the linear input range even further for use with TileCal pulses.

With these changes the receiver system can handle all possible input signals from both of the calorimeter types.

Further results

Discussions during the tests also led to the decision to raise the cut-off voltage of the receiver's output stage to 3.2V, resulting in 3V at the Pre-Processor input, after cable attenuation, rather than at the receiver output like in the initial design. This can be considered to be a rather theoretical step to better comply to specifications, though, as the maximum digital value of the Pre-Processor's FADCs corresponds to 2.5V at the input, the region above being not visible to the trigger[5].

Concluding, with the changes resulting from the Heidelberg integration tests, the Receiver System fulfills all its tasks inside its specifications, and Bunch Crossing Identification is not only feasible, but straightforward with the algorithms of the Pre-Processor. The Pittsburgh group had a very successful Production Readiness Review of their receiver system in the meantime.

[5]but some voltage limiting is needed for the input of the operational amplifiers on the AnIn

5.2 The Receiver system and the Pre-Processor at the CERN Testbeam

After correct interfacing and functionality of the combined Pre-Processor/Receiver system was ascertained in Heidelberg, the next goal was to integrate the Pre-Processor into the full analog chain starting at the calorimeters. One custom VME crate carrying one PPM was moved to the H8 test beam at CERN, where a Receiver Board was already present. With signals from the TileCal calibration system, the signal chain was examined using an oscilloscope and results from digitization by the PPr's FADCs were read out from the PPrASIC.

5.2.1 Setup of the system

Signal source

Principally the test beam setup including the calorimeters was present as introduced in section 4.3.1 starting on page 37. As the following work was done during a week of SPS machine development, though, no beam was available. Furthermore the LAr calibration system was not ready for use, resulting in the TileCal calibration system to be the only option as signal source.

The TileCal calibration system uses direct charge injection into the front-end electronics to simulate real TileCal pulses. The amplitude and time placement of the pulses is programmable and they resemble pulses from energy deposition of particles extremely well, with the difference of having a slightly faster rise time. They were provided at a rate of ∼1Hz. A single arbitrary analog signal cable from the calorimeter was sufficient for the tests, as the calibration system was programmed to produce identical signals on all channels.

All cables and the TileCal Patch Panel used to route the signals to the Receiver System were production prototypes.

Receiver system

A single Receiver Board resided in a 9U crate, together with its rear-mounted Transition Board and a TileCal Patch Panel.

Of the changes decided during the testing in Heidelberg only the component exchange lowering the time constant of the shaping stage from 15ns to 5ns was implemented on the Receiver Board. With the VGA daughter boards' input voltage range unchanged and thus not suited for the full amplitude range of the TileCal signals, pulses saturating the TileCal trigger tower sums could not be used.

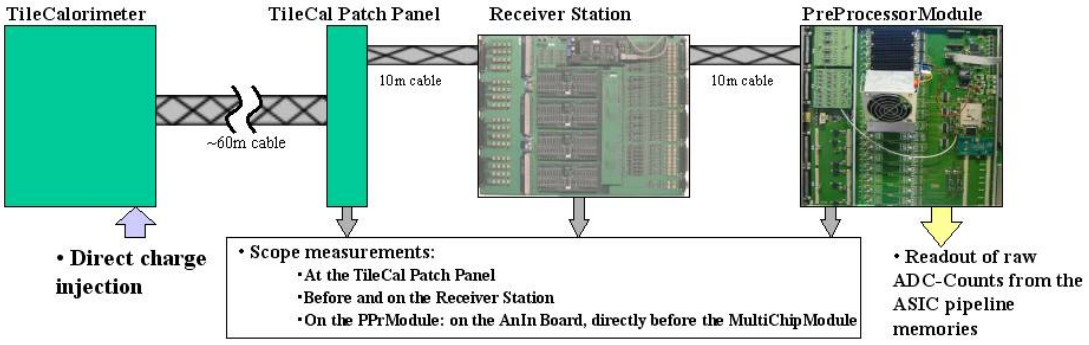

Figure 5.8: Test setup of the analog chain from the TileCal to the Pre-Processor

The Receiver board was operated passively with default settings, that is unity gain for all channels, and using a Remapping Board which directly and straightforwardly routes all channels through the Receiver as in the tests in Heidelberg. Hence signal amplitude and position on the cables was left unchanged by the Receiver, and it was mainly included in the setup to have the full analog signal chain in place and to verify all prior test results in the realistic environment of the test beam and with a PPM.

Pre-Processor

One PPM with two AnIn boards and four MCMs was used for the test, plugged into a custom VME crate together with a crate controller cpu, a TCM and a TTCvx[6] module. The crate was placed directly on a desk without a fanning unit, therefore a small fan was directly mounted onto the PPM for MCM cooling. One of the AnIn boards had custom modifications to provide a trigger, which is described below.

The PPM was controlled over the VMEbus using a standalone software.

Timing and trigger

While it is technically possible to get timing and trigger signals synchronized with the TileCal calibration system, it was not known during preparation which systems would be available for the test beam stay. Accordingly the Pre-Processor was equipped to supply its own clock and trigger to be able to run independently in a self-triggering mode.

The TTCvx automatically uses an internal 40 MHz clock in absence of an external clock. This clock was transmitted to the TCM using an optical link

[6]providing the clock, encoded onto a TTC signal

Figure 5.9: From left to right: Pre-Processor Crate, front of the Receiver crate(with the Receiver and the TileCal Patch Panel), back of Receiver crate(with the Transition Board)

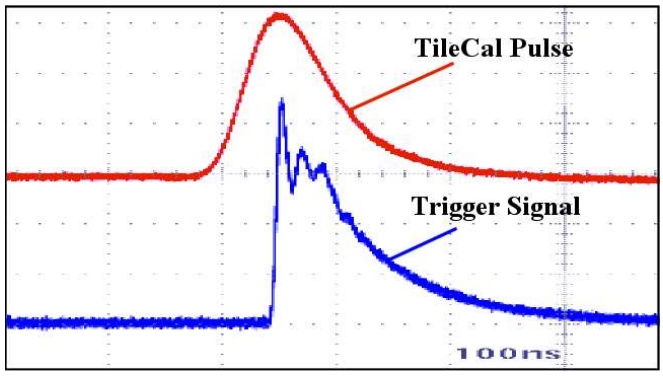

Figure 5.10: TileCal calibration pulse and trigger signal created by the AnIn

and distributed from there on the backplane to the PPM. As the clock was not synchronized with the calibration pulses, the position of the ADC digitization points on the signals was floating from pulse to pulse.

Since the pulse rate of ∼1 Hz was very low compared to the length of the internal PPrASIC pipeline memory, 3.2μs, it was impossible to read out digitized pulse data without a trigger. In order to be fully self-sufficient, one AnIn board was modified to provide a trigger signal directly to the RemFPGA. The programmable thresholds of the AnIn responsible for generating the external BCID were used, with an 'or' operation over all channels, and the resulting signal(see figure 5.10) was converted into a 'clean' Level-1 Accept, a square pulse with a length of 25ns, by the RemFPGA.

5.2.2 Tests and results

Verification of the signal path

Firstly measurements of the analog signal chain were done with an oscilloscope at all accessible points downstream of the TileCal patch panel, most prominently before and after the Receiver Board and at the input of the AnIn boards of the PPM.

The goals of this measurement were to check for correct signal levels, polarity and pinning at all connectors, verify the routing of boards and panels and lastly examine the pulse shape and amplitude. The general purpose was to identify and sort out any potential issues in preparation of a combined Level-1 Calorimeter Trigger test beam.

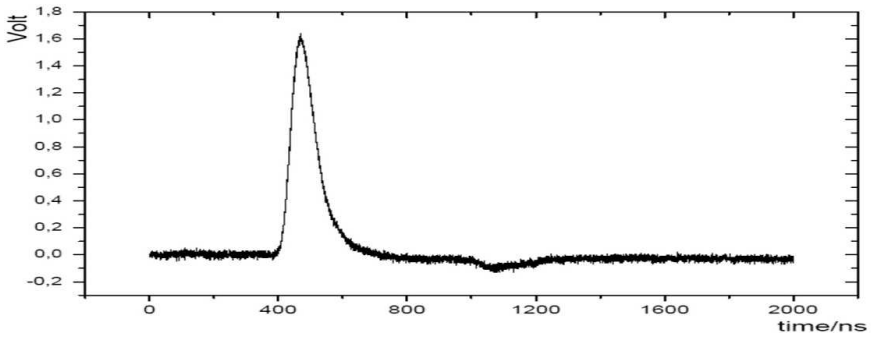

Figure 5.11: TileCal calibration pulse, measured at the input of the AnIn board

The pulse mostly used can be seen in figure 5.11 and roughly corresponds to an energy of 250 GeV. While this should result in 2.5V at the PPM input in a calibrated system, the Receiver Board was run with unity gain, thus not compensating for the signal attenuation over the cable or doing any calibration. The signal was preceded by an oddly shaped pseudo pulse in a variable time distance, having about one third of the pulse amplitude(not visible on the figure). According to the TileCal group this was a leak of charge into the system from the bunch-crossing counter reset signal, which is used as a timing frame to position the calibration pulse. Visible on the figure, though, is a dent in the baseline $\sim$600ns after the pulse. This is believed to a be an echo of the signal due to improper termination of the 60m cable from the TileCal to the PatchPanel. This supposition is supported by the position of the signal dent exactly corresponding to the expectation of such an echo, and its shape.

Apart from these effects the calibration pulses were clean, very stable and matching the recorded pulses from a 2001 test beam which had been used for tests in Heidelberg.

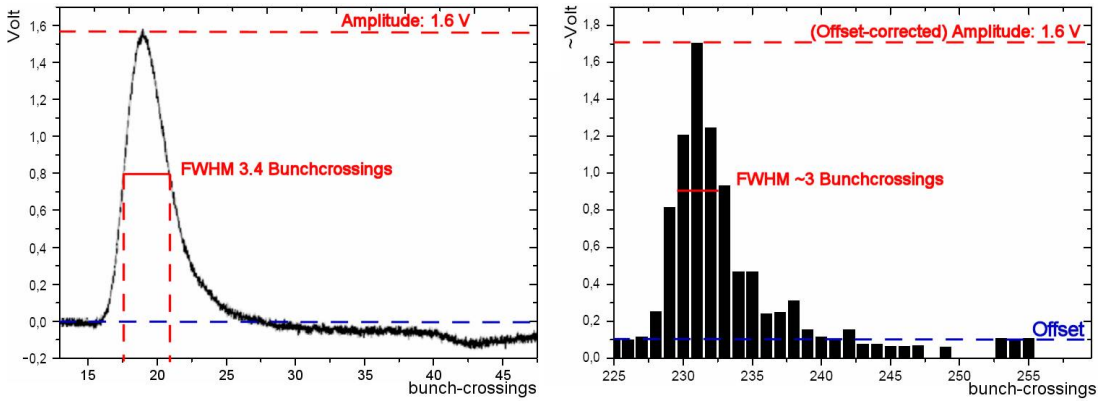

Figure 5.12: Comparison of analog pulse(left), measured before the AnIn, and digital readout of the PPrASIC(right)

The signal path from the TileCal Patch Panel to the input of the Pre-Processor MCMs was fully understood and no problems were encountered, all systems working and complying to their specifications.

Readout of ADC counts

With the analog signal chain verified digital data was looked at. The results of the digitization on the MCMs are not only used as input to the BCID algorithms, but are also buffered in a pipeline memory of the PPrASIC. This allows for readout of these results to document the data processing of accepted events. For this standalone test, the self triggering mode was used to initiate the readout. The data was then buffered again in the RemFPGA awaiting to be accessed over VME.

Figure 5.12 shows an example of ADC results acquired in this way. The data was converted from ADC counts to Voltage[7] and plotted offline, and is shown in comparison to the analog measurement of the pulse at the input of the PPM.

After subtracting the pedestal a very good agreement of the amplitude can be found, and the analog pulse shape and FWHM[8] can be identified. Fitting the two pulse measurements however is impeded by bumps on the falling edge of the digital plot.

Principally the readout of digital data was successful, but the data suffered from this unknown effect.

[7] using average ADC characteristics

[8] Full Width Half Maximum, the full pulse width at half its maximum amplitude

5.2.3 Conclusions

The whole analog signal chain from the Hadronic Tile Calorimeter to the Pre-Processor system had been verified for a sample of channels in a realistic setup and environment. Moreover calorimeter signals where transmitted, processed and digitized using final ATLAS components for the first time.

The achievement was not without flaws, though, as the readout of digital ADC results of the calorimeter pulses showed errors. It was later discovered that these are caused by a timing issue of the RemFPGA firmware. The ADC data is copied internally from a pipeline which is continually overwritten to another buffer to await readout via VME. During this copying process, timing problems lead to bit errors of the data. This could be confirmed as the source of the problem using a simulation of the RemFPGA.

As the bit errors could be allocated to the the readout chain, the real-time data path was cleared for tests including digital processing of the whole Level-1 Calorimeter Trigger.

Chapter 6

Tests of the processing chain of the LVL-1 Calorimeter Trigger

In order to sort out and fix problems and bugs of the L1 Calo Trigger subsystems and of their cooperation, a slice test had been planned. A slice test is an experiment in a lab environment with a small portion of a system(slice). The intention is to assure functionality of the slice to later integrate it as a whole into the full system. In this case the slice is the L1 Calo Trigger, part of the ATLAS Trigger system. Prior to and in preparation of an attempt of this test several smaller segments of the L1 Calo Trigger have been tested.

Because of logistical reasons, the modules being built in Mainz, the Jet/Energy-Sum Processor always was the first candidate of the two L1 Calo Trigger Processors for combined tests with the Pre-Processor. Two integration tests were done in Mainz, a pilot run using the Pre-Processor Test System and a second one shortly after the first PPM was available. Both were strictly focused on the real-time data path, the goal being to verify the Pre-Processor's LVDS output. All links towards the processors use the same technology, hence successful data transmission to the JEP principally validates the whole real-time data interface of the Pre-Processor.

The next step was to recheck the results gained from the JEP tests with a CP module at the Rutherford Appleton Laboratory(RAL) in England, again looking first at the LVDS data. Furthermore with DAQ hardware and experts available, one further focus was integrating the PPM services software into the ATLAS DAQ environment, to switch to the Online Software for combined control of the trigger system and replace the PPr standalone control programs. Lastly a combined test of all L1 Calo Trigger subsystems was attempted at the RAL.

6.1 Pilot integration of the Pre-Processor Test System and the JEM

While LVDS output had been read out and tested by the Pre-Processor Test System, no attempt had been yet made to pass it to one of the Processors. Hence the PPr test system was brought to Mainz for integration with the JEP in November 2003. As none of the modules involved were production prototypes[1], the goal was to verify the functionality of the systems for the longest possible section of the real-time data path in principle, instead of concentrating on the actual modules and their interfaces.

6.1.1 Test setup

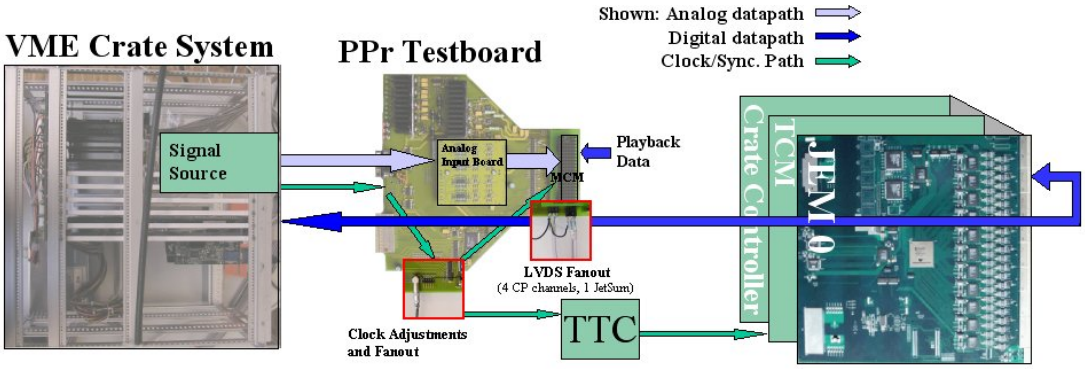

Figure 6.1: Diagram of the test setup

All systems were set up principally identical to standalone tests, allowing the use of existing hardware, firmware and software. The connection of the Pre-Processor Test System and the JEM was made using fanout of LVDS signals, thus leaving existing data paths intact. One issue needing attention, though, was clocking the systems. A common clock being necessary, some module had to supply a master clock.

Pre-Processor Test System

In contrast to the Receiver-PPr tests described in the previous chapter the Pre-Processor Test System was set up exactly like for standalone tests, its functionality staying fully intact. The connection to the JEM was established by the fanout

[1] not taking submodules like the MCM into account

of signals rather than opening an existing data path. As data sources analog signals from the signal source and digital test data injected via the MCM's playback memory were available. The closed control and data paths of the system stayed in place, making readout of data with the VME crate system possible.

The LVDS fanout was implemented directly at the output of the MCM for all three channels, one being a jet channel and the other two carrying data for the CP. A custom built LVDS cable was used to connect to the JEM, its short length of 1.5m making precompensation circuitry as on the PPM unnecessary.

Jet/Energy-sum Module

The Jet/Energy-sum Module used was an earlier prototype(JEM 0) than the one described in section 3.2.4 on page 30. Its functionality principally the same, the main difference is the use of only one FPGA for the JEP algorithms. As a result they could not be loaded at the same time, and only the Energy-sum algorithm was available for the test. The JEM was controlled with a Concurrent Technologies crate controller and a TCM supplied the clock coming from the TTC system.

Timing, control and readout

Components of the ATLAS TTC system, a TTCvi and a TTCvx board, were used to provide the clock for the JEM. Both boards were run passively and supplied an internal 40 MHz clock. Two options were now available, either clocking the Pre-Processor test board with this clock, or to supply the the test board clock to the TTC system. As the analog signal source can not be synchronized to a clock, only vice versa, it was necessary to use the test board clock in order to get correctly timed analog signals. But as this clock is derived from a 100kHz sync signal using a frequency scaler it was unclear if it is stable enough for the LVDS links. A fallback option was to use the internal 40MHz quartz of the test board and digital test data only, though.

Control and readout of the setup was split into two halves, both systems using independent paths and software. Most importantly this meant that no combined readout was possible. As a result of the fanout both systems could theoretically read out the LVDS links at the same time, but the start of readout could not be synchronized. Additionally LVDS data was first buffered in FPGA memories in both systems, and the cycle to read them back surpassed the memory lenght by far, resulting in staggered data snippets instead of a continuous stream that could be matched.

Data was read out from three places:

- The LVDS signals going into the VME crate system

- Input Spy Memories of the JEM

- Intermediate Spy Memories of the JEM, containing the total transverse energy sum

Data format

Three LVDS channels were individually provided to the JEM, one being a real jet element, the other two principally being channels intended for the CP. Resulting from the design of the PPrASIC it is only possible to freely set the output of the CP channels using playback data, as BC-muxing and BCID can be switched off for these, but BCID and jet element summing for the jet channels can not. 10-bit data words are send by the LVDS serializers, so the cluster channels can be used to transmit fully arbitrary 10-bit values using the playback memories as data source. With BCID and BC-mux activated, a 9-bit jet element energy value protected by one parity bit is sent via the jet channel, and an 8-bit energy value plus one BC-mux bit[2] and one parity bit is sent on the CP channels. Supplying a CP channel to a JEM results in the BC-mux bit being interpreted as the least significant data bit. So the JEM interprets the data value as a number twice as high as a CPM, plus a single count if the BC-mux bit was 1.

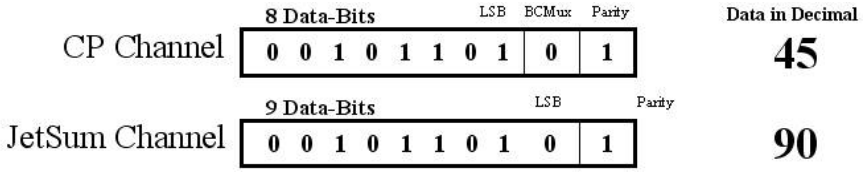

Figure 6.2: Example of a CP channel 10-bit word, and its interpretation by the JEM

All readout consisted of raw data files of a certain length, with the data words written out for every bunch-crossing.

The data content of the channels during the tests with BCID logic enabled are referred to as ADC counts in the following, and not energy values, as no calibration was done and the lookup table in the PPrASIC handed results through unchanged.

[2]to be able to de-mux the data in the CP

6.1.2 Tests and results

Connectivity

All systems had been set up and correct operation was certified by short standalone tests. The PPr test board clock, generated by a 40MHz quartz crystal in absence of an analog signal, was provided to the TTCvx board, distributed further from there. A phase lock between the JEM and the PPr clocks was achieved, being the first time the TTC system was used for a combined system and with an external clock, which is comparable to operation in ATLAS with the external LHC clock.

All three LVDS cables were connected to the JEM, and a stable LVDS lock of the links was achieved. Furthermore correct pinning of the modules' connectors could be confirmed.

While being a preparation for the following tests, having a stable lock of LVDS serializers and deserializers using a common clock was a first success by itself.

Purely digital data transmission

Using looped and uniform digital data patterns as input to the system, event to event correlation is not necessary and the the missing ability to do a combined readout is no limitation if no debugging is needed. CP channels were used for the tests to have the above mentioned full freedom of data content.

At first 10 bit raw data patterns were injected with the PPrASIC playback memory, bypassing BCID logic. The correct patterns were read back from the JEM input spy memories. Next patterns resembling ADC results of calorimeter pulses were played back and BCID enabled. Again data was first read from the input spy memories of the JEM, and the correct BCID results, values of ADC counts corresponding to the peaks of the played back pulses, were found. As data was now fully processed in the PPr and hence parity protected, it was visible in the energy sum spy memories (data failing the parity check is zeroed in the JEM input stage).

Tests using analog data

As the tests using digital test data were a full success, the signal source was changed to the analog one. A ramp pattern was used as test signal, created from HEC calorimeter pulses recorded at the testbeam. The undershoot of the signals was cut off to bunch the steps of the ramp closer together, one pulse every $150ns$ (6 bunch-crossings). The ramp had 9 steps and was repeated every $2\mu s$ (80 bunch-crossings).

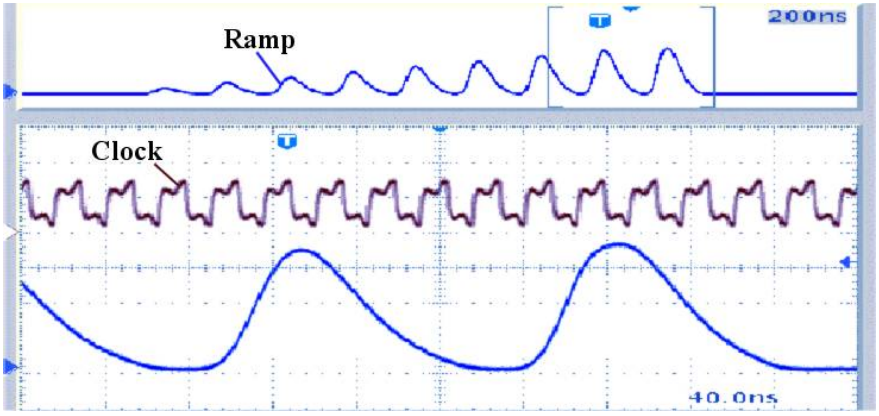

Figure 6.3: Pulse ramp used for the tests with analog input, the clock signal is shown as reference in the magnified region

The first success while using this analog signal was that the LVDS links stayed stable, since as mentioned in the test setup the clock generated from and in sync to the analog signal has considerable jitter. The setup was run for about 30 minutes while data was taken.

Data-taking was not optimal as generally readout of the two systems was not synchronized, and no automated run could be started for the JEM. Data was first taken from the JEM, initiating the dumping of spy memories into a file by hand, resulting in low statistics. Afterwards the PPr test system was set to write out its memory continually resulting in a larger data set. Only data from the two cluster channels is presented here, as the BCID results of these are in the same bunch-crossing. The jet element channel was looked at but as it is send one tick later due to the summing it does not appear in the same total transverse energy sums.

Results of the tests with analog input data

As there is no direct correlation between the data samples, they can only be analyzed using the total statistics and not on a per event base. The first plots, shown in figure 6.4, histogram all events read out by the two systems. The upper histogram shows ADC counts directly read from the real-time path using the Pre-Processor test system. As 8-bit data words plus the BC-mux bit of the CP channels, which was constant, were interpreted as 9-bits of data the resolution and resulting bin size is 2 ADC counts. The two channels were summed offline. The lower histogram shows all data read directly from JEM spy memories containing the total transverse energy sum. These data includes scale bits, resulting

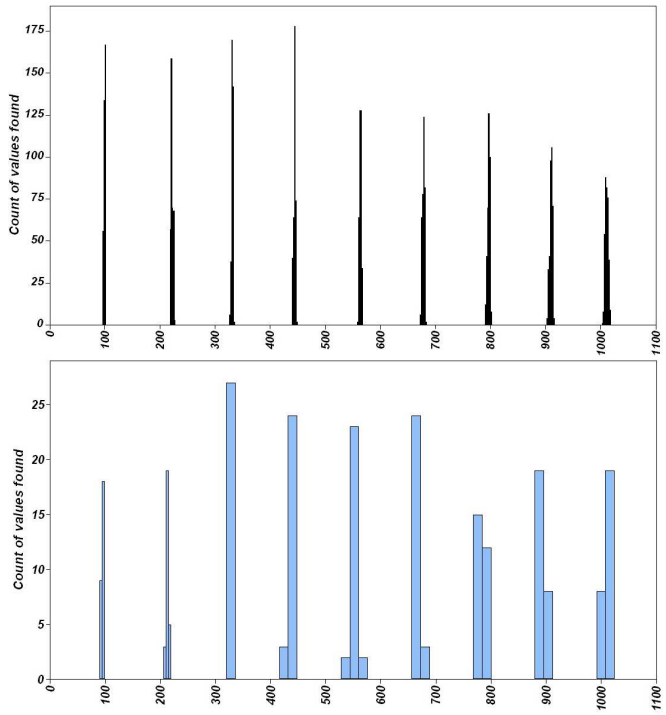

Figure 6.4: Data read from the Pre-Processor Test System(upper graph, summed offline) and the JEM

in different resolutions depending on the energy range of the sum. The bin size is correspondingly 4 ADC counts in the range up to 255 ADC counts, and 16 for the rest of the histogram.

On first glance the histograms show a very good resemblance. A distribution of values around the peak is clearly visible, resulting from jitter of the analog amplitude and the sampling points of the FADCs. It is reasonably thin, though, and the the peaks are clearly separated. On closer inspection one can notice that all peaks on the PPr test system histogram seem to be shifted to slightly higher energies compared to the JEM readout. Some small effect of that kind is to be expected as the energy sums in the JEM are rounded, but a more thorough examination was necessary.

As the peaks on the histograms corresponding to the steps of the analog input signal are nicely separated with no noise in between, i was able to assign all values to a certain step and calculate the mean ADC count value read out for each. Figure 6.5 shows a comparison of these mean values from both systems. The standard deviation of the mean values is below 1% and hence too small to be shown on the plot, which further indicates correct assignment of the values.

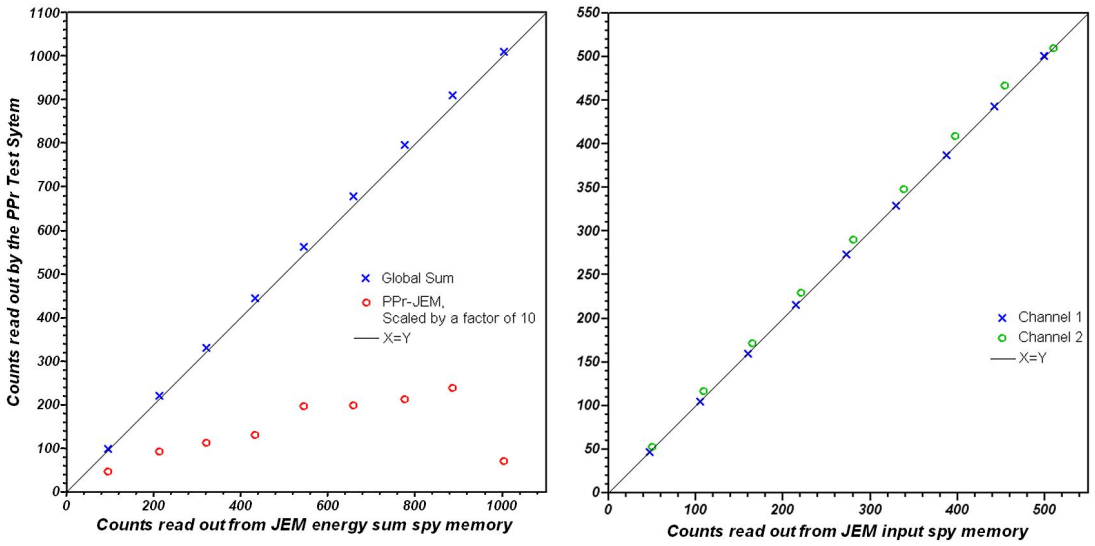

Figure 6.5: Direct comparison of readout from the JEM and PPr test system, on a per energy step basis

The left graph clearly shows that the PPr test system on average read higher values out for all signal steps, the difference between the two readouts is also shown scaled up by factor of 10.

The graph on the right is a comparison between readout of the PPr test system and of the input spy memories of the JEM, both per channel and not summed. It is apparent that channel 1 perfectly fulfills our expectations of identical mean values from readout, and channel 2 is the source of the issue, which is consistently carried over into the sums.

As the data is parity protected it is very unlikely that this effect is caused in the digital part of the system, moreover as faulty bits would with all probability not lead to a consistent increase in the data value of roughly 3% over most of the range[3].

6.1.3 Interpretation and conclusions

The integration tests of the Pre-Processor Test System and the Jet/Energy-sum Processor were a big achievement, despite them not being flawless. The test setup was successfully run with a master clock derived from the signal source, corresponding to the LHC clock in ATLAS and distributed via the TTC system, which is a quite realistic environment. The whole real-time data path from the

[3]the highest value is around the maximum digital output of the ADCs

analog source up to the total transverse energy summing of the JEM was tested, and connectivity and proper communication of the systems was easily achieved.

Analysis of the raw data read out from the setup with analog input revealed an irregularity. This is most likely localized in the analog part of the test system and further testing attributes it to the signal source, as the data was taken consecutively and a change to the test system resulting in a slightly altered amplitude of the signal is quite possible in between.

Concluding, both the PPr test system and the JEM functioned fulfilling the requirements and expectations and a first pre-slice test including final PPr components had been very successful.

6.2 Combined operation of the Pre-Processor Module and the JEM

The next, natural step up from the integration of final Pre-Processor components with a prototype JEM was a test of a sub-slice including production prototypes of ATLAS modules only. This test was done in Mainz, as soon as the PPM was in a sufficiently finished state which was in July 2004. A LVDS board, providing precompensation for and driving the 15m LVDS cables had just been loaded with components and the main focus of the experiment was on testing and debugging the LVDS output of the PPM, as no LVDS data sink suitable for the PPM was available in Heidelberg.

6.2.1 Test setup

In contrast to the prior integration in Mainz, the hardware setup was a real slice of the ATLAS Level-1 Calorimeter Trigger. It corresponds to the final setup in ATLAS, one part of the system taken out and assembled on a smaller scale.

Pre-Processor

The Pre-Processor system consisted of a custom crate with a VME 64xP backplane, housing a homebrew crate controller, a TCM and one PPM. The PPM was fully equipped for a limited number of channels, including two AnIns, six MCMs and one LCD board, the LCD board only partly loaded with components for the needed channels. The firmware for the RemFPGA on the PPM was in a non-final state with the readout path not active.

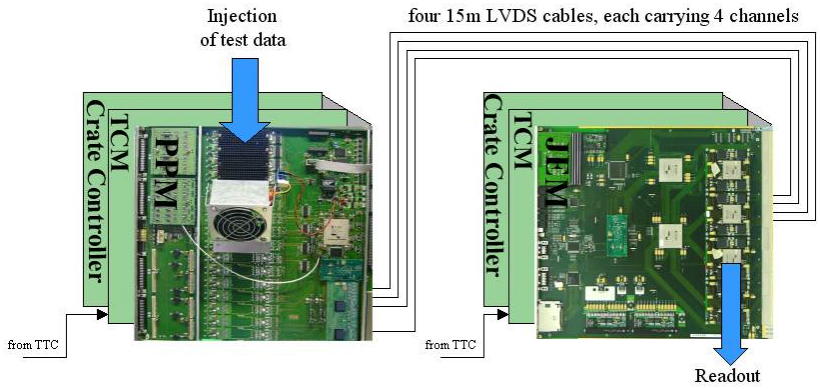

Figure 6.6: Sketch of the test setup

Jet/Energy-sum Processor

The JEP setup in Mainz was left unchanged, the used modules being one JEM 1, a concurrent crate controller and one TCM.

Timing and Control

A TTCvx and TTCvi module simulated the TTC system of ATLAS, the TTCvx supplying the master clock which was transferred to the TCMs with optical links, and from there further distributed on the backplanes.

The JEM was initialized, controlled and read out by the Online Software, a component of the ATLAS DAQ system. As the PPM services had not yet been fully integrated into the Online Software, a standalone software was used for the PPM.

6.2.2 Test procedures, proceedings and results

Types of measurements

As the emphasis was on the quality and stability of the LVDS links, testing the parameters of the precompensation and the suitability of the LCD board's FPGAs as cable drivers, readout of actual data played a minor role. Digital test patterns were injected into the PPrASIC with the playback memory and send to the JEM using 15m LVDS cables, corresponding to the maximum length in ATLAS. The 12 CP channels were always run bypassing BCID and BC-mux logic, and correct parity bits were included in the patterns loaded into the playback memory. The six jet element channels always have BCID enabled.

The main source of information were automatic tests of incoming data in the JEM input modules, implemented in the firmware of the input FPGAs, and respective error counts which could be read out. In this way high statistics can be accumulated.

Achieving a stable LVDS link

The first test pattern replayed was the trivial one, continuous zeroes as data. It was expected that the LVDS serializers automatically send a synchronization pattern upon startup and at each reset of the MCM. The LVDS cables where plugged into the JEM and a reset issued to the running MCMs, but the LVDS deserializers were not able to lock upon the signal. Powerdown and powerup of all modules, with cables plugged in, did not yield better results.

Sending repetitive non-zero data immediately after powerup of the system finally led to the LVDS serializers and deserializers locking on some channels. The non locking channels were later found to be wrongly routed on the LCD board. Switching to zero data on a locked link did not cause a loss of link, switching to non-zero data achieved no link on non-working links. If a link was established, it even recovered from removing and plugging the cable back in.

Extensive testing work has been done on this issue, it still being not fully understood. The problem probably is the startup sequence of the MCM, though. A missing feature of the PPrASICs used in the test did not send an arriving reset request on to the LVDS chips. Apparently if the MCM was reset without cleanly resetting these chips, they sometimes entered a non-functioning state from which they could not recover. The correct LVDS reset was already included in the new MCMs with new PPrASICs which were being produced in an engineering run at the time of the test, so use of a workaround was planned. But some vulnerability of the setup was probably also present, as the prior tests although using the PPr Test System and a JEM 0 but the same MCMs and thus PPrASICs did not suffer from this issue.

In summary stable links could be established on the 12 CP channels and one JEP channel, the other five JEP channels having routing problems on the uncompleted LVDS board.

Parity and data checks

The work was concentrated onto the working channels, and parity errors examined. The JEM input modules have an internal parity error counter which can be read out. First checks revealed a large number of parity errors on some channels, in the order of 1 in 10^5. Cabling of the system was verified, and the PPM was powered down and up, not solving the issue. It was decided to finally change

the reset scheme of the MCMs in the standalone software controlling the PPM to separate the LVDS link lock and parity problems.

After this change the LVDS connection was stable but the parity error counter of the jet element channel saturated instantly. The opinion was that we do have some problems with the creation of correctly parity protected data on that channel, and it was decided to have a closer look at CP channels with non-zero data first. The playback memory was filled with a pattern to result in a ramp on the CP channels with BCID disabled, ramping the energy up by increments of 1 count from 0 to 255, and the JEM firmware was adjusted to identify and check this pattern.

As a first success, the system was left running for 30 minutes, resulting in $\sim 10^{11}$ transmitted values without a single error detected on all 12 CP channels used. To verify the test procedure an error was introduced into the pattern, and rightly detected by the JEM.

In the meantime it was discovered that during implementation of the new startup and reset sequence a mistake had been made, setting the register controlling the data format of the jet element channels to default. The default is 10 data bits without parity protection, explaining the high error count. The initialization software was fixed and parity failures reexamined.

With the ramp pattern and the parity bit enabled, no parity errors where detected on the jet element channel. Next pseudo-random data was written into the playback memory, in this case meaning a random pattern with the length of the memory, 256 values, was generated, provided with a correct parity bit and replayed in a loop. The result was, again, a high number of parity errors on the JEP channel, at least of the order of 1 out of 10^4, while the 12 CP channels operated flawlessly. Several random patterns were generated and used, resulting in seemingly different error rates, but the problem persisted.

Due to time constraints, testing was ceased at this point.

6.2.3 Conclusion

The experiment was able to point out some issues of the setup, f.e. the vulnerability to a non-optimal startup sequence and parity problems using random data on the jet element channel. The first issue, problems with the the LVDS link stability, was solved during testing and did not occur again. Not all expected channels had data on them during the test, but this could be later attributed to the partly finished LCD board and was fixed by fully equipping it with components and completing the routing inside its FPGAs.

But the occurrence of a high number of parity errors on the jet output persisted during most of the tests, and is not fully understood. While a fixed and simple pattern like the ramp led to positive results, random data input at a high

frequency lead to a high number of bit errors. The quality of the LVDS signals on the cables was comparable to the CP channels, making bit errors during transmission unlikely. It was believed that a timing and clock distribution problem on the PPM or inside the RemFPGA is responsible for the issue, the LVDS clock flanks not sitting nicely on the the data stream from the PPrASIC leading to bit errors during serialization of the data or on arrival at the LCD FPGAs. It is unclear why only the jet channel is affected, though. As many changes and improvements to the hardware and firmware were already planned,the PPr components used partly being in an unfinished state, a reevaluation of the situation was postponed to a later date.

As a conclusion, correct transmission of digital data over the LVDS links with 15m of cables was achieved for the large majority of channels, strongly hinting at the general viability of the LCD board as cable driver, including the precompensation circuitry. It was evident, though, that the PPr group needs a way to read out the LVDS data streams in Heidelberg, to be able to conduct more thorough tests including a larger number of patterns and fully random data after the test beam[4].

6.3 Pre-Processor/Cluster Processor and the full system tests

The following testing work was conducted at the RAL in England at the end of July 2004, and in contrast to the tests in Mainz the goals were twofold. One priority was sending LVDS data from the PPr to the CP similar to the JEM tests, checking and debugging the real time data path, the other one migrating the control of the PPM from the standalone software to the Online Software environment of ATLAS DAQ and to examine the readout path via the DAQ system.

Not having been present during these tests, preparing the Level-1 trigger installation at the test beam at the same time, I compiled the following short section on the accounts of participating members of the PPr group[19]. It is mainly included to complete the coverage of tests of the Level-1 Calorimeter Trigger processing chain.

[4]time constraints did not allow for that before the test beam

6.3.1 Combined PPr-CP test

Setup

The test setup consisted of two crates both having one Concurrent Technologies(CCT) crate controller and one TCM equipped, one crate housing the PPM the other one the CPM. A single LVDS cable was used to connect the systems, resulting in four LVDS channels and up to eight trigger tower channels due to BC-muxing.

Timing was done by TTC modules with the clock distributed to the systems using optical links. The CPM was controlled using the Online Software, while HDMC[5] was the main method to control the PPM. HDMC was used as a standalone software, but as it is also the interface to the PPM used by the Online Software this was still one big step towards integration of the PPr into the DAQ system.

LVDS data transmission

Data was successfully loaded into the playback memory via HDMC and transmitted to the CPM over the LVDS links. Connectivity and LVDS link lock did not pose any problems. The data was received properly by the CPM on the correct channels. Some parity errors were detected, though, and were not fully understood during the test. They were probably attributed to problems of correctly starting and synchronizing all playback memories, though, and RemFPGA firmware changes were planned to solve this issue.

Software integration

First steps were taken to integrate the PPM software into the Online Software environment. After a large time investment the system was set up successfully, and the PPM software was able to read from the Online Software database. Reaching this stage was a notable achievement, but much work, especially concerning initialization of the PPM, was still needed.

In summary the LVDS data transmission was quite successful, but showed that the RemFPGA firmware was still in an preliminary stage. Integration of the PPM into the Online Software environment had been started, also with first successes, but mostly presented useful pointers to areas needing more work.

[5] a Hardware Diagnostics, Monitoring and Control Software

6.3.2 Full Level-1 Calorimeter Trigger Setup

Test Setup

The system used resembled a small scale setup of the whole Level-1 Calorimeter Trigger, plus the interface to the DAQ system. One PPM, one CPM and one JEM were placed in crates with CCT crate controllers and TCM modules. Readout Drivers(RODs) for the readout data of the L1 Calo Trigger and TTC modules providing the clock complemented the testing environment.

Operation of the PPM

Most of the time available for this test was spent trying to achieve proper operation of the PPM using the Online Software for the first time, as this was required for the combined test beam. The registers of the PPrASIC were changed by the Online Software using a method called 'read modify write', meaning that the values are first read back, and then only the necessary bits are written instead of the whole register value. As read back from the PPrASIC was not working correctly in the RemFPGA firmware and the firmware fallback option was also bugged, this method produced erroneous configuration data in the PPrASICs.

Finally, when the the problem outlined above had been pinned down after two days of work, a workaround was implemented in the software and testing was able to proceed.

LVDS data transmission

The first results of LVDS transmission to the CPM and JEM generally looked reasonable, but one MCM produced large numbers of parity errors. To further test the LVDS link to the JEM, a ramp as test data was envisioned similar to the prior PPM-JEM test in Mainz. Unfortunately as a remnant from standalone tests of the JEM using a DSS[6] the JEM expected a ramp from 0 to 512 in steps of 1, which the PPM is unable to supply with its playback memory depth of 256 samples. Resulting from the very harsh time limitations severely worsened by the work that had been needed to achieve proper operation of the PPM, tests concerning the real time data path had to be halted at this point.

Readout tests

A check of the read out of the PPM using a rear mounted G-Link Module was strictly planned before the combined test beam. The signal from the G-Link Module looked promising on the oscilloscope, and the cable was connected to a

[6]Data Source and Sink, a module for standalone tests of the JEM and CPM

ROD. No data arrived at the ROD, though, and several attempts were made to solve the issue. In the end the connection was working with an optical link, the cable used before seeming to be broken.

Conclusion

While the above tests did not produce many results going beyond prior ones, some important steps had been made like confirming the basic readout functionality of the PPM and integrating its control into the Online Software. Admittedly the final full slice test verifying the whole processing chain of the Level-1 Calorimeter Trigger was not achieved, and the system could have been better prepared for the test beam. But the condition of the subsystems was workable for the test beam environment and many issues were discovered that could be fixed in the weeks following the tests at the RAL.

Chapter 7

The Level-1 Calorimeter Trigger at the CERN Test Beam

The last endeavor to evidence a working Level-1 Calorimeter Trigger system described in this thesis is the combined run at the H8 ATLAS test beam at the CERN. In this context combined not only means the L1 Calo Trigger, but the full spectrum of ATLAS detector types and a Level-1 Trigger Setup including the Muon Trigger and the Central Trigger Processor as well as parts of the DAQ system. The main L1 Calo Trigger involvement at the combined test beam was from the 6th of September to the 11th of October 2004, the SPS running in LHC comparable 25ns mode during the last week. Additionally a pilot installation week had been carried out in the beginning of August 2004.

As fully successful integration of the L1 Calo Trigger subsystems in a lab environment had not been achieved yet(see chapter 6), the installation and operation of the system at the test beam was no trivial task. A feasible mode of operation was reached, though, and first results became available during the time of writing.

7.1 Setup

The goal of the test beam setup at CERN was to encompass all detector and Level-1 Trigger systems of ATLAS, and emulate ATLAS on a small scale. The desired maximally realistic environment was not only important for tests, but sticking to the design of ATLAS also saved preparation work as the setup had already been specified in full detail.

7.1.1 Analog systems

Beam, Calorimeters and front-end electronics

The setup of the calorimeters and the front-end electronics is described in section 4.3.1 starting on page 37 in more detail, as are beam characteristics. Only the outline will be repeated here.

The beam at the H8 test beam mainly consisted of secondary particles created by shooting the SPS accelerators's proton beam(with a typical energy of 400 GeV) onto a target. Beam optics in the H8 line allowed to select type and energy of secondary particles arriving at the detectors. A virtual point of interaction can be imagined in the center of a magnet system, where the beam could be bent to hit different regions of the detectors.

One electromagnetic LAr barrel module and three hadronic TileCal barrel modules were installed in the beam line, with the TileCal being behind the LAr module seen in the direction of the beam. The geometrical setup of the calorimeters closely resembles a fraction of ATLAS, in respect to the virtual point of interaction. A shared ϕ/η-coordinate system of all modules can be established, with the unbent beam centered around $\eta = 0.4$ and $\phi = 0$. The most interesting η-region, where the beam was for the majority of the time, is from 0 to 0.8 and covered by both calorimeters. One difference to ATLAS was the placement of the modules in ϕ, though. They were centered around the beam line and the LAr barrel module covered $-0.2 < \phi < 0.2$ and the TileCal modules $-0.15 < \phi < 0.15$. As the trigger towers are uniformly sized 0.1×0.1 in ϕ/η in the above mentioned η region, this resulted in the LAr module being four trigger towers high in ϕ, while the TileCal only had a height of three and the towers are overlapping by half with the LAr ones.

The full front-end electronics were installed for the TileCal, resulting in three cables to the trigger control room each carrying signals from trigger towers of a fixed ϕ and all η values, while the two Tower Builder Boards needed to fully cable the LAr module were not continuously present during the tests, and only three cables, occupied like the TileCal ones, were available leaving at least one ϕ-row of trigger towers unconnected.

Receiver System and channel mapping

The driving principle for the setup of the analog signal cables, the Receiver boards and the used Remapping Board was to be able to roughly cable all digital systems as one would do in ATLAS[1]. Hereby the first requirement for the analog signal cables to the Pre-Processor is that each carries signals from an area of 4×4 trigger

[1] see [13] for details on L1 Calo cabling in ATLAS

towers in $\eta \times \phi$. Furthermore the calorimeters at the test beam are very thin in ϕ and long in η, while a single JEM or CPM requires the array of input data to be long in ϕ. A second goal was to be able to leave all analog cabling in place after the initial installation, without needing to recable between runs with the TileCal, the LAr calorimeter or both.

A setup complying to these requirements was achieved based on one 9U crate with two fully equipped Receiver Boards. One of these boards was used for the three cables from the TileCal modules, the second one for the three LAr cables. The boards were both prototypes predating the Receiver System Production Readiness Review, and as such the change to the shaping stage, being the most vital one, was the only one resulting from the Receiver tests in Heidelberg that was implemented(see section 5.1 on page 45 for details). One important notice is that the Receiver Boards were always run using default parameters, thus operating with unity gain. They did not compensate for the signal attenuation over the cables, as they would do in ATLAS. As a result all energies measured by the L1 Calo Trigger were ∼35% too low.

Concerning Remapping Boards many options had been considered and tested at first, but a single type has been used for all data-taking. This type is needed in ATLAS for parts of the Hadronic End Cap calorimeter and is called ID 16[2]. It was chosen as it coincidentally also fulfills the above requirements of the test beam. Trigger Tower channels are grouped into the Receiver output cables in correctly ordered arrays of 4×4 and it effectively switches η and ϕ when used for the barrel modules. Luckily[3] the channel mapping inside the cables is comparable for the LAr and TileCal barrel modules, thus the same Remapping Board could be used for both Receivers. As only three cables, carrying a total of three ϕ bins, were laid from each calorimeter to the receiver, the cables to the Pre-Processor were only 75% occupied.

In summary, the relevant regions of the two calorimeters were mapped onto input cables to the Pre-Processor comparable to the final ATLAS setup, and only these cables had to be moved to assign TileCal or LAr channels to a PPM. Concerning combined data-taking with the calorimeters, it had to be remembered that the L1 Calo Trigger interpreted η as ϕ and vice versa.

7.1.2 Level-1 Calorimeter Trigger hardware

Pre-Processor

A single 9U crate with a VME 64xP backplane was used to house the Pre-Processor system. For compatibility reasons two crate controller CPUs were

[2]see [20] for the description of and information on all LAr remapping board types

[3]no TileCal specific Remapping Boards existed at the time of the tests

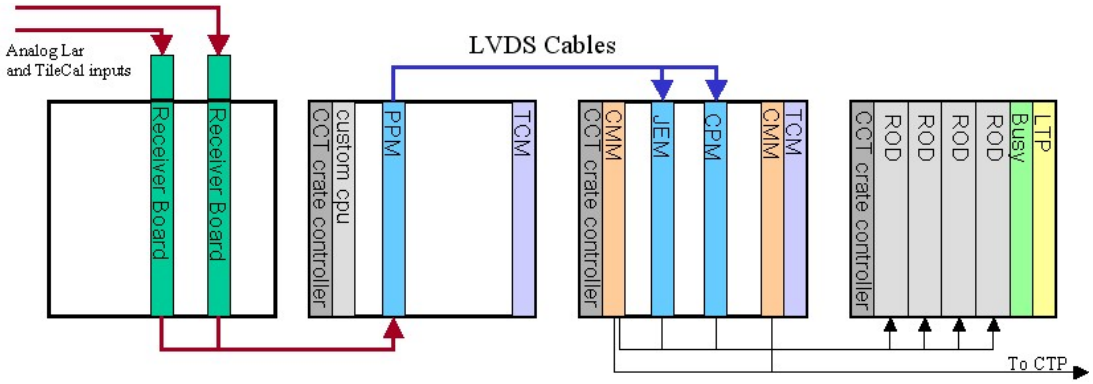

Figure 7.1: Sketch of the crate setup, TTC not shown

installed, a homebrew one based on a standard PC motherboard and a Concurrent Technologies(CCT) crate controller. One TCM and most importantly one PPM completed the setup. A second PPM and two rear-mounted G-Link modules were also tested, but not used during data-taking.

The analog signal cables coming from one of the Receivers, either carrying LAr or TileCal channels, were straightforwardly connected to the inputs of the Pre-Processor. As mostly trigger towers of η from 0 up to 0.8 are of interest[4] and each cable carries signals of an area 0.4×0.4 in $\eta \times \phi$, two cables sufficed to connect one Receiver Board to the Pre-Processor. As the PPMs have four input connectors, a single PPM was able to process all significant channels. During a high η scan of the LAr barrel module the cables were shortly moved on the Receiver output connectors, resulting in a visible region of $0.4 < \eta < 1.2$ for the LAr channels.

Cluster and Jet/Energy-sum Processors

One CPM and one JEM were installed at the test beam, in a shared crate with one CCT crate controller, one TCM and two CMMs. The LVDS cables coming from the PPM were connected based on the ATLAS cabling scheme, as well as all outputs of the crate: the G-Links from the processors to the RODs in the readout data path and connections from the CMMs to the CTP in the real-time data path.

[4] η is used in detector nomenclature here and in the following, despite it being interpreted as ϕ by the trigger due to the Remapping Boards

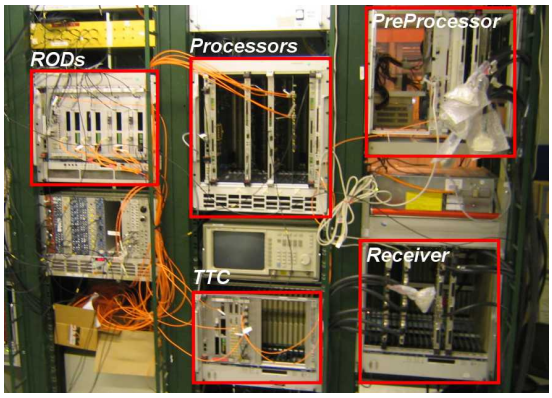

Figure 7.2: Front view of L1 Calo Trigger and Receiver crates

7.1.3 Timing, Trigger, Control and Readout

Timing and trigger signals were provided by the CTP group and fanned out to all other groups. The L1 Calo Trigger used a pair of 6U TTC modules to encode those signals and distribute them to the TCMs via optical links, from where they were further distributed on the backplanes of the crates. For most of the test beam period a mock-up CTP, basically a delayed beam trigger from scintillating counters, provided the Lvl1 Accept signals to initiate readout, but at the end a real CTP was also fed with trigger objects from the CPM and JEM to produce Lvl1 Accepts.

For the readout of data from the L1 Calo Trigger a 6U crate with 4 RODs was installed and connected to the system. Further modules in the crate were a CCT crate controller, a Busy module[5] and a Local Trigger Processor(LTP)[6].

All control of the system during data-taking runs was done using the Online Software environment, a component of the ATLAS DAQ system. Data was written out and histogrammed offline as well as directly histogrammed online, both by use of a Monitoring package.

7.2 Installation and operation of the Pre-Processor

While the Pre-Processor did have its share of problems during installation and operation, it was of course not the only subsystem of the L1 Calo Trigger having issues. Nonetheless describing all these would go beyond the scope of this document and thus this section is focused on Pre-Processor related items. Prob-

[5]to issue and manage 'pause' commands during a run
[6]a local substitute for operation without the CTP

lems are not only outlined in the following to document the massive work that went into solving them, but also to point out resulting restrictions for the the acquisition of data.

7.2.1 PPr Crate and crate controllers

The initial crate installed for the PPM was a custom crate with an integrated small power supply, comparable to the crate of the PPr Test System but with a VME 64xP backplane. The first problem that was found and tracked down were voltage dips on the PPM and the backplane when the module was switched on, leading to instable operation. In the end a heavy duty 9U crate, designated for use in the final experiment, was brought to CERN and the PPM was running stable. While the issue had been circumvented by the new crate with a more stable power supply, this is only true with a single module. To be able to operate 16 PPMs in one crate, it will have to be solved, and work regarding this was underway in Heidelberg in parallel to the test beam.

The next goal was to initialize and control the PPM using the Online Software and the CCT crate controller. While all testing in Heidelberg had been done using the custom crate controller, from the DAQ point of view use of the CCT cpu was highly desired at the test beam as it was netbooted from a shared Online Software partition ascertaining that all systems always run with the same version. But due to timing or VME bus issues, occurring intertwined with the above mentioned power problems which complicated the bug finding, the CCT crate controller was not able to perform all necessary operations. A workaround was set up, using the Heidelberg custom crate controller for some initialization tasks after startup of the PPM and the CCT cpu for the operation of the running module.

In the mean time the processor setup had also reached a functional state.

7.2.2 Real-time data path

First transmission of LVDS data went flawlessly between the CPM and PPM, while the JEM encountered a small but significant number of parity errors on some channels. The issue was identical to the observations of the PPM-JEM tests in Mainz(see section 6.2.2 on page 71), with the parity errors occurring with random data, like input from the calorimeters, but not when a simple fixed pattern like f.e. a ramp is inserted with the PPrASIC playback memory. One possible cause for this, timing problems of the LVDS signals, was already discussed in the above mentioned tests and one newly found issue of the JEM, some voltages which were too low on the module, was also considered. The

problem was not solved and will have to be thoroughly examined after the test beam.

Sending sensible LVDS data based on incoming calorimeter pulses also was not possible at first, but this could be tracked down to horribly wrong settings for the PPrASIC FIR filter that had slipped into the configuration files. As a solution trivial coefficients have been inserted and used, effectively disabling the FIR filter. Although the problem was caused solely by the settings, and the filter is fully functional, it is not strictly required for the test beam runs and this solution was the easiest and fastest one.

One further problem, though located in the control path, influenced the real-time data flow. Limitations of the Phos4 chips on the MCMs lead to a high vulnerability of the startup and initialization phase. With a fully equipped PPM this often caused several MCMs to not function correctly. The decision was made to reduce the amount of channels used, and limit the coverage to an area two trigger towers high in ϕ, instead of the three available on the cables. Accordingly eight of the seemingly more stable MCMs were plugged onto the PPM, and seven of these were found working. The last one was not able to produce any sensible LVDS data during the whole test beam period, but the problem appeared not to be the MCM itself. Exchanging it did not change the behavior of that channels and it seemed to be attributed with the position on the PPM. The three LVDS channels were switched off in the LCD board, as the cause was and could not be found in the test beam environment. While a possible hardware solution to the Phos4 problems was discovered later during the test beam period, the running system was not modified or changed.

With a sufficient subset of channels working, a huge and tedious effort had been put into setting the DAC offsets of the AnIn boards to result in in identical pedestals in the digital data. The PPM then was ready for data-taking runs, although still with occasional parity errors in the connection to the JEM.

Towards the end of the test beam period the real-time data path was successfully extended from the calorimeters all the way to the CTP. Though small restrictions existed due to problems on most modules, the principal functionality was achieved, and a major milestone reached.

7.2.3 Readout and DAQ

No working connection between the rear-mounted G-Link modules and the RODs could be established, leaving PPM readout unaccessible. This problem will have to be examined and solved following the test beam.

Readout of the processors and the CMMs was achieved with some effort, though, and all data taken is based on this.

7.3 Preliminary results

In the following a short summary of some early results of the Level-1 Calorimeter Trigger group at the H8 ATLAS combined test beam will be presented. As no analysis of the data was possible before the completion of this document, the last data-taking runs were done just one week before the submission date, all results and interpretations have to be considered very preliminary. The data was just filled into the histograms 'as is'.

7.3.1 Noise measurements

One of the first successful measurements examined the noise coming from the calorimeter modules and all analog electronics. The pedestal of the AnIn boards was moved up to result in 120 counts and the distribution of values digitized by the ADCs was measured and read out by the CPM, with no analog signal cables connected to the PPM at first. Cables from both the hadronic TileCal as well as the electromagnetic LAr calorimeter, not carrying any signals, where then connected and the distribution measured again. Plots for two representative channels are shown on figure 7.3, with 2000 events taken for each plot. The data read were ADC results with 10-bit resolution directly sent to the CPM bypassing the BCID logic.

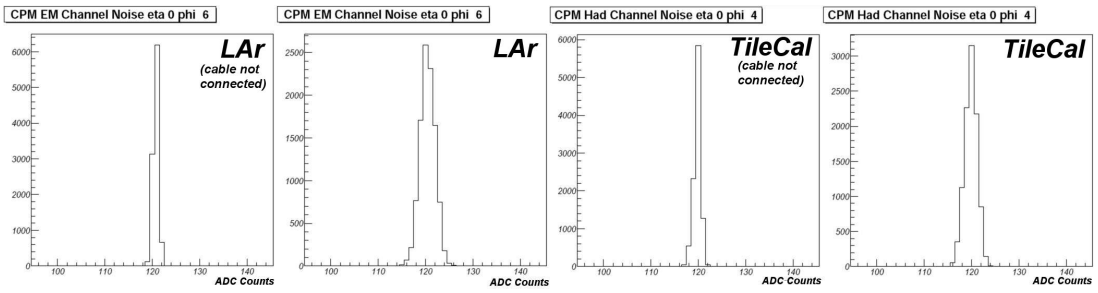

Figure 7.3: LAr and TileCal noise measurement, pure PPM noise(left one of each pair) and with calorimeter and pre-PPM electronics noise

Interpretation

It can be easily discerned from figure 7.3 that the full swing of the noise measured with cables not connected is about three ADC counts for both channels. This increases to seven counts with connected LAr cables, and six counts with connected TileCal cables. The conversion factor of ADC counts to voltage is

in this case, with the full 10bit value corresponding to 2.5V, about 2.5mV per count. But this only applies to the input voltage to the PPM. Getting a correlation to GeV is more complicated, as the Receiver Board was set to unity gain. Firstly this means that the channels are not calibrated, and all values have to be considered rather rough, as operational amplifiers in the electronics have slightly different gains for all channels. But most foremost the amplitude loss over the cables is not compensated, with the total of 80m of analog signal cables having an attenuation factor of roughly 0.65. Hence in a fully calibrated system, the noise from the detector and front-end electronics would be amplified by about 50%, while the noise from the Receivers own operational amplifiers, from the PPM DACs and the quantization error would stay the same. As we only do a rough approximation, though, the front-end electronics and Receiver Board noise is expected to be negligible compared to the calorimeter and pre-amp noise.

So it is safe to assume that the amplitude of the noise inherent to the PPM is less than 5mV which corresponds to 500 MeV[7]. Furthermore the total noise amplitude on a TileCal or LAr channel can be expected to be no more than ≈12mV in a calibrated system, that is ∼1.2 GeV. For comparison, as 8-bit energy values are given out by the BCID logic, the resolution of BCID results is 1 GeV.

7.3.2 BCID of TileCal calibration pulses

As the normal SPS beam structure is quite different from LHC, there was no correlation between the clock used for the system and the occurrence of beam particles and thus analog signals for most of the test beam period. Together with the problems of non-functioning channels in the PPM and parity errors at the JEM input, data taken was hard to interpret. Hence a period with low energy tertiary particle beam(∼2 GeV) was used to check and verify time offsets of the different subsystems and the functioning of channels making use of the TileCal calibration system. Uniform signals with an amplitude of 1.5V at the Pre-Processor input were created in a fixed correlation to the clock.

At first the DAQ readout offset settings were set to catch the raw 10-bit ADC results of the pulses, bypassing BCID, in the five bunch-crossings that can be read out from the CPM. The resulting plot for one channel is shown to the left in figure 7.4. The x-axis is the time in 25ns ticks, but it is not continuous as only the consecutive readout results where placed in the histogram. For each readout five samples of the calibration pulse, centered around the peak can be seen, the consecutive readouts separated by one empty bin. Apparently the calibration signals are very uniform. The plot to the right of figure 7.4 shows the situation after the BCID logic has been enabled and the readout time offset

[7] 2.5V≈ 250 GeV

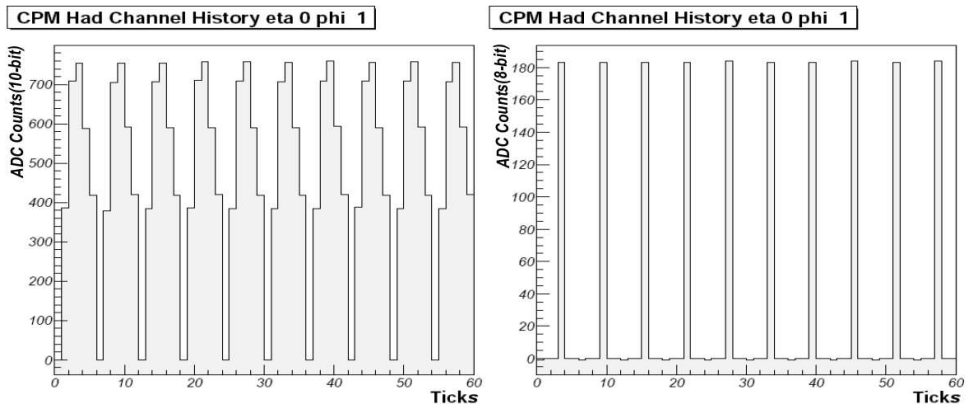

Figure 7.4: Time slices readout from the CPM, bypassing BCID(left) and with BCID(right)

was adjusted back for normal operation. A single 8-bit value remains from each pulse representing the corresponding energy determined by the BCID.

The next figure, 7.5, shows plots of the total energy sum readout from both the CPM and JEM. While a distinct peak is visible corresponding to the uniform calibration signals, the energy sum over all channels in the JEM is much lower. This strongly hints to some channels having constant parity errors at the JEM input, as data with parity errors is zeroed. These channels had already been identified using the parity error counter of the JEM input modules, but the counter has to be refreshed by hand it saturated too quickly to be able to

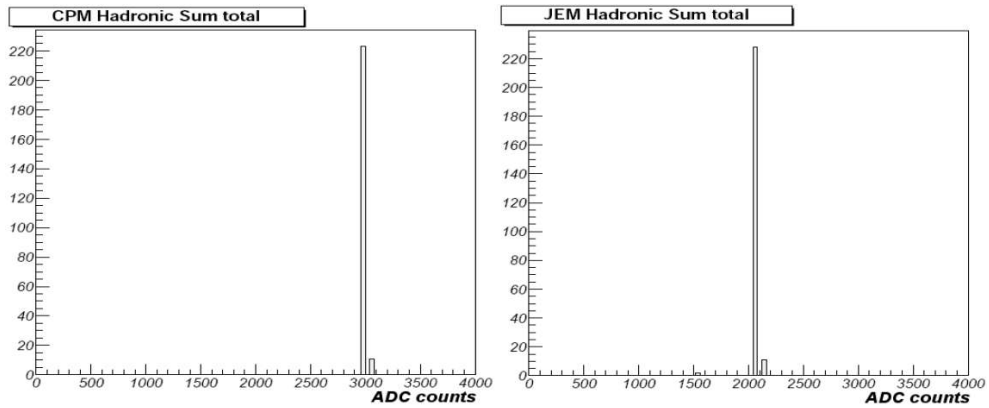

Figure 7.5: Readout of the total energy sum over all channels in the CPM and JEM

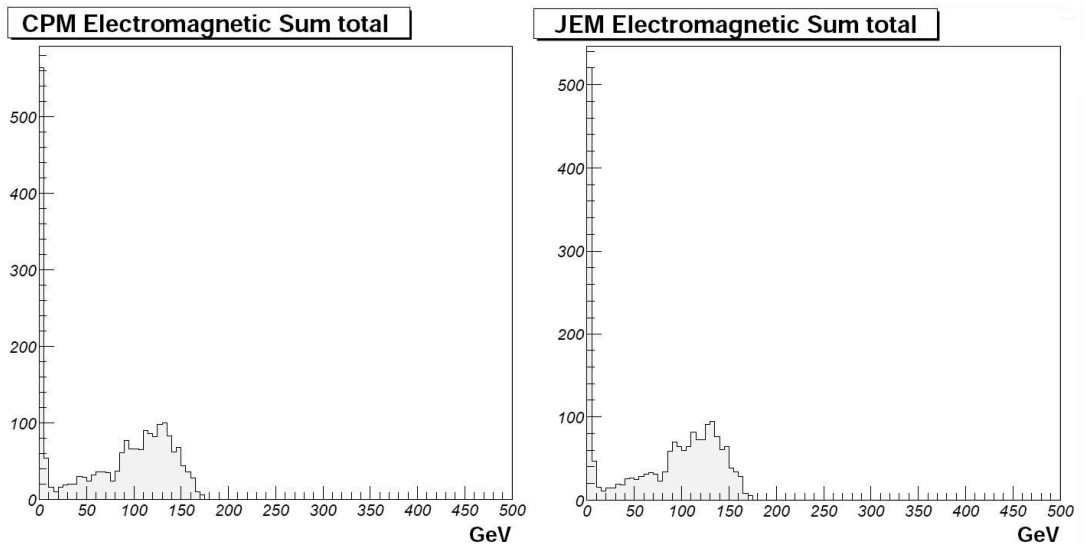

Figure 7.6: 250 GeV beam events read out from the CPM and JEM

determine if parity errors are constant or only appear at a moderately high rate.

Some CPM data also had parity errors arriving at the CMM, but this could be fixed with minor timing adjustments.

7.3.3 Beam energy measurements with the CPM and JEM

A next step, after the verification of settings described above, was to conduct a data-taking run during a period with a 250 GeV beam at $\eta = 0.55$, primarily consisting of pions intermixed with about 10% electrons. All non functioning channels had been masked out on both the JEM and the CPM and the signal pedestals were subtracted by use of the PPrASIC Lookup Table. Figure 7.6 compares the event histograms of the two processors, while the energies read out from the JEM and CPM are compared on a per-event basis in figure 7.7. Data shown is from the electromagnetic LAr calorimeter barrel module.

Interpretation

The first thing to remember for interpretation of the plots is that the system was not calibrated. The attenuation of the signal on the cables from the front-end electronics alone reduces the amplitude by about 35%. Furthermore as the signals float in respect to the digitization points the highest ADC count is generally lower than the actual amplitude. Thus the position of the main peak of the energy distribution, consisting of electron events, seen by the L1 Calo Trigger is

quite explainable. The peaks at the left edge of the plots on figure 7.6 are false BCIDs caused by noise. These were read out when a trigger was produced by a particle which then hit the calorimeter outside of the region visible to the L1 Calo Trigger setup. The thick tail of the distribution towards low energies is not that easily explainable. Effects playing a role, though, are the composition of the beam, mainly being pions, and some electrons occasionally hitting an edge of and losing energy in more than one trigger tower.

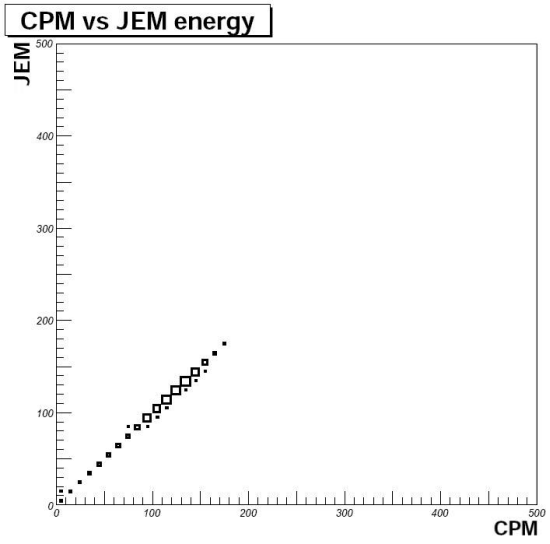

Figure 7.7: Correlation between energies of events read out from the CPM and the JEM

The comparison of energy read out from the JEM and CPM on figure 7.7 shows a very good correspondence. Though this is to be naively expected as both system receive the same parity protected digital data, it nicely shows that the problems in the realtime path, though some have not been solved, do not affect the data-taking anymore. For example the absence of points with significant energy in the CPM and none in the JEM give proof that the channels used did not suffer from parity errors upon arrival at the JEM. The line of points directly below the diagonal is to be expected as in some cases the reduced granularity and resolution of the jet elements lead to slightly lower energy sums in the JEM.

In summary, the plots evidence that the system now was in a good shape for the oncoming week of 25ns beam, and sensible readout could be produced.

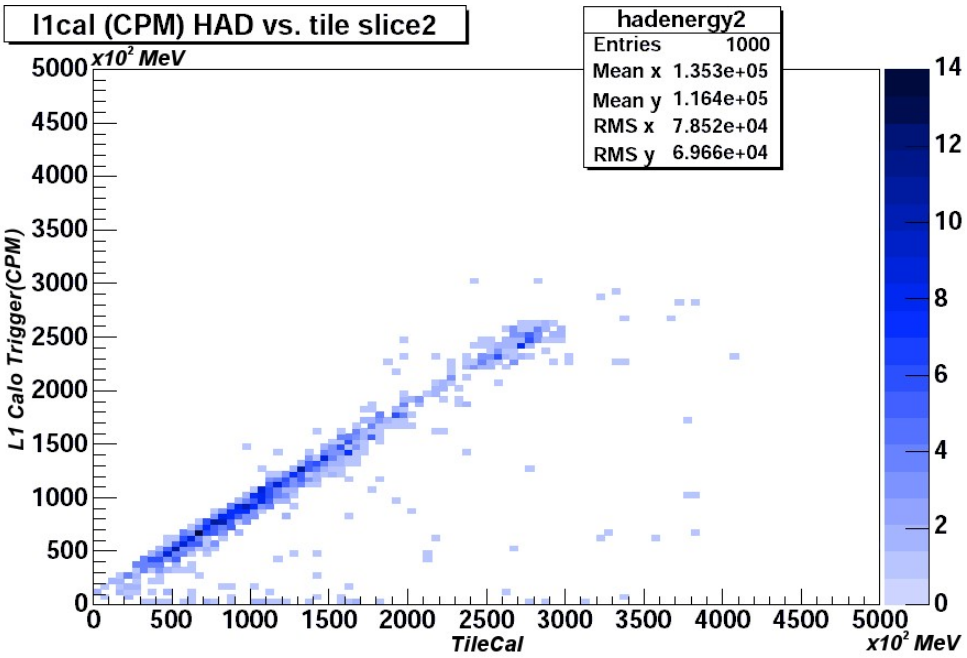

Figure 7.8: Energy readout from the L1 Calo Trigger vs energy reconstruction by the TileCal

7.3.4 Comparison of TileCal and L1 Calo Trigger readout

The plot in figure 7.8 shows data taken during the last week of the test beam period. During that time the SPS machine was run in an LHC-like mode, with the beam structured into bunches in 25ns intervals. Data-taking runs were done combined, with all system, the detectors and the full Level-1 Trigger integrated.

The presented data is taken from the TileCal during a run with 300 GeV primary proton beam. Shown is the energy sum over all channels read out from the CPM plotted against the energy reconstructed in the TileCal modules, for 1000 events.

Interpretation

While at least now a clear coincidence between the signals and the clock existed, the L1 Calo Trigger system was still in no calibrated state. Hence the units on the vertical axis are somewhat artificial, and only very roughly correspond to about 10^2 MeV.

The large majority of the 1000 events on the plot lie on a straight line, showing a nice linear correlation of the two energy readouts. The irregularities visible are

a result of two effects. Firstly while the readout from the TileCal had access to the the whole geometric size of all modules, the CPM only received data from two of the three TileCal Modules and respective ϕ rows, due to the limitations described in section 7.2 on page 81. The beam having a wide spread, parts of the energy of some protons were deposited in the region invisible to the L1 Calo Trigger, resulting in the data points below the linear expectation on the plot. The few events with zero energy in the L1 Calo Trigger originate from a wrong time slice being read out, f.e. possibly caused by a misplaced BCID due to the lack of time and BCID calibration.

Overall the combined data-taking run was a huge success evidencing that the L1 Calo Trigger sees and processes correct energies, and that the combined event readout with the DAQ system is working.

7.4 Test beam conclusions and outlook

The results presented above are only a small selection, and a much larger number of achievements had been made and milestones reached at the test beam. In summary at first all L1 Calo Trigger subsystems had been combined successfully, supplying reasonable data and results. The Online Software was used to control the modules, and the L1 Calo Trigger was integrated into the combined test beam partition, allowing common runs with the CTP, the muon system and the detectors. Huge progress had been made in connecting the L1 Calo Trigger to the DAQ readout system and the CTP, where many problems were identified and overcome.

Moreover a prototype CTP was successfully supplied with trigger objects from both L1 Calo Processors, multiplicities of clusters passing energy thresholds from the CPM and of jets from the JEM, as well as the thresholds passed by the global energy sums of the JEM. A Lvl-1 Accept was generated from this data and used to initiate readout, thus the entire functionality of the real-time path has been verified in general.

Concluding, it has been shown that the L1 Calo Trigger is able to meet its requirements, and is principally fully functioning. Some problems have been identified in all the modules, though, and demonstrated that quite some work on the individual modules will still be necessary before commissioning of the system.

Chapter 8

Summary and outlook

The previous chapters described tests to integrate the Level-1 Calorimeter Trigger Pre-Processor not only into the Level-1 Trigger but the whole ATLAS environment. The Pre-Processor has an analog interface to the calorimeters as well as digital interfaces to the processors and readout systems, its main task being to determine the transversal energy corresponding to the deposition in the calorimeters and providing it to the processors in the correct time slice.

The first testing block given account for was the work done and successes achieved in integrating the Pre-Processor into the analog signal chain. A laboratory test together with the Receiver System was not only very successful, but also provided valuable information to finalize the design of the Receiver Boards. Both systems were taken to the CERN test beam, and while issues were discovered with the readout, the real-time path from the calorimeters through the Receivers into the Pre-Processor was found to be fully functioning.

The next endeavor described was joining the Level-1 Calorimeter Trigger subsystems together and assembling the digital processing chain. While many issues were discovered a number of them already have been overcome and none are insurmountable. Even though it has yet not been reached, the tests and results can be considered first successful steps towards the goal of a fully working Level-1 Calorimeter Trigger.

The combined test beam run of the Level-1 Trigger and ATLAS detector components was only shortly introduced, as no thorough analysis of the data has been possible so far. Nonetheless the preliminary results point at a generally quite successful outcome. The full signal and processing chain from the calorimeters to the CTP, where a Lvl-1 Accept signal was generated from data provided by the Calorimeter Trigger, and back to the readout of the calorimeters was confirmed. Moreover event readout from the Level-1 trigger and the TileCal showed a very good correlation, evidencing proper data transmission, processing and readout.

In summary the Pre-Processor performed its tasks generally successful. Issues

of the PPM and the LCD card were discovered, but most solutions are already on the way and a second version of the prototypes of these boards had been envisioned from the beginning in any case. Some problems like f.e. the occasional high parity error rates of the transmission to the JEM will still have to be thoroughly examined, though, and it became obvious that the firmware for the PPM is in no final state yet. One further point made clear is that a dedicated test bench for the PPM is needed and additionally will be vital for the production tests.

After an immensely busy period severely impacted by the time constraints caused by the fixed test beam period, there will now definitely be more time to study and solve the problems, before further integration tests and the Production Readiness Review of the PPM are done. This is even more so as the vital components of the system, the MCMs, are already fully finalized and functioning, and became ready for production in parallel to the tests described in this document.

First parts of the Pre-Processor will be installed at the CERN in 2005, and the whole Level-1 Calorimeter Trigger is planned to be fully commissioned in 2006.

Bibliography

[1] CERN Positioning Metrology and Surveying Group, http://est-su.web.cern.ch/est-su/LHC_SU.htm

[2] Abstract for ATLAS, CERN Database of experiments('Greybook')

[3] W. Cottingham, Derek Greenwood: *An Introduction to the Standard Model of Particle Physics*, 1998

[4] *ATLAS Detector and Physics Performance Technical Design Report*, ATLAS TDR 14, 1999.

[5] *ATLAS High-Level Trigger, Data Acquisition and Controls Techincal Design Report*, ATLAS TDR-016, 2002.

[6] W.E. Cleland, Bin Liu, J.Rabel and G.Zuk: *Receiver/Monitor System for the ATLAS Liquid Argon Calorimeters*, ATL-AL-EN-0043, 2003.

[7] Ulrich Pfeiffer: *A Compact Pre-Processor System for the ATLAS Level-1 Calorimeter Trigger*, 1999.

[8] *ATLAS Level-1 Trigger Technical Design Report*, ATLAS TDR-12, 1998.

[9] *Prototype Cluster Processor Module for the ATLAS Level-1 Calorimeter Trigger*, 8th Workshop on Electronics for LHC Experiments, Conference Contributions pages 256-260, 2002.

[10] Stefan Rieke: *JEM1: Status and Tests*, Level-1 Calorimeter Trigger Joint Meeting, June 2004.

[11] ATLAS Test Beam Homepage, http://atlas.web.cern.ch/Atlas/GROUPS/GENERAL/TESTBEAM/2004/.

[12] Frederik Ruehr for the Heidelberg ATLAS PPr group: *Lvl1 Calorimeter Trigger Analog Cabling and Channel Mapping for the H8 Combined Testbeam*, 2004.

[13] L1 Calo Group: *Cable Mappings and Crate Layouts from Analogue Inputs to Processors*, ATL-DA-ES-0036, 2004.

[14] Karsten Penno: *A Test Environment for the ATLAS Calorimeter Trigger*, 2002.

[15] Frederik Ruehr: *ATLAS Integration Test of the PPr Testsystem with the Receiver Station*, 2004.

[16] H. Stenzel: *ATLAS Test Beam Measurements of Analogue Level-1 Calorimeter Trigger Tower Signals*, 2001.

[17] Vladimir Savinov, *Pitts Tests of the Receiver/Monitor Stations for the ATLAS Calorimeters: Part 1*, ATL-AL-EN-0049, 2003.

[18] Bill Cleland, Univeristy of Pittsburgh, email correspondence.

[19] Florian Foehlisch and Kambiz Mahboubi, private conversations and email correspondence.

[20] V. Paolone: *Remapping Boards for the ATLAS Liquid Argon Receiver System*, ATL-AL-EN0046, 2003.

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Glossary of Abbreviations

ADC	Analog-to-Digital Converter
AnIn	Analog Input Board, a submodule of the PPr
ATLAS	A Toroidal LHC ApparatuS
BCID	Bunch-Crossing Identification
BC-mux	Bunch-Crossing Multiplexing, for transmission to the CP
CERN	European Organization for Nuclear Research
CCT	Concurrent Technologies, a brand of crate controllers
CMM	Common Merger Module, merging results of the processors
CP	Cluster Processor of the L1 Calo Trigger
CPM	Cluster Processor Module
CTP	Central Trigger Processor, making the final L1 Trigger decision
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition System
DFM	Data Flow Manager of the DAQ
EF	Event Filter, the third trigger stage
FADC	Flash Analog-to-Digital Converter
FPGA	Field Programmable Gate Array
HDMC	A Hardware Diagnostics, Monitoring and Control Software
HEC	Hadronic Endcap Calorimeter, using LAr technology
HLT	High Level Trigger
JEM	Jet/Energy-sum Module
JEP	Jet/Energy-sum Processor of the L1 Calo Trigger
L1 Calo Trigger	The ATLAS Level-1 Calorimeter Trigger
L2SV	LVL2 Supervisor, part of the LVL2 Trigger
LAr	Liquid Argon, referring to ATLAS calorimeter types
LCD	LVDS Cable Driver board, a submodule of the PPr
LHC	Large Hadron Collider
LVDS	Low Voltage Differential Signaling
Lvl1 Accept	Signal that an event has met the level-1 trigger criteria
MCM	Multi Chip Module, a submodule of the PPr

PLL	Phase Locked Loop
PPM	Pre-Processor Module
PPr	Pre-Processor of the L1 Calo Trigger
PPrASIC	The chip performing all digital processing of the PPr
PRR	Production Readiness Review
RemFPGA	Readout Merger FPGA, a chip on the PPM
ROB	Readout Buffer
ROD	Readout Driver
RoI	Region of Interest
RoIB	Region-of-Interest Builder of the LVL2 Trigger
SFI	Sub Farm Input of the High Level Trigger
SFO	Sub Farm Output of the High Level Trigger
SPS	Super Proton Synchrotron
TBB	Tower Builder Board, summing LAr cells into Trigger Towers
TCM	Timing and Control Module
TileCal	The hadronic Scintillating Tile Calorimeter
TTC	Timing, Trigger and Control
VGA	Variable Gain Amplifier of the Receiver System
VMEbus	Versa-Module Euro, a crate backplane bus system

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