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Rate Metering for the ATLAS Experiment

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Rate Metering for the ATLAS Experiment

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Zusammenfassung

Rate Metering ist ein wertvolles Instrument zur Überwachung der Kalorimeteraktivität des ATLAS Detektors auf Triggerebene. Im Rahmen dieser Diplomarbeit wurden die dort zu erwartenden Signalraten studiert und ein Testaufbau entwickelt, um die Funktionalität der Hardwareimplementierung des "*Rate Metering and Histogrammings*" auf dem Präprozessor-Modul des ATLAS Level-1 Kalorimeter Triggers zu überprüfen. Eine Simulation der auftretenden Physik unter Einbeziehung aller Detektoreigenschaften wurde benutzt, um die Signalraten im späteren Experiment zu untersuchen und deren Abhängigkeit von Schwellenenergien zu bestimmen. Zielsetzung des Testaufbaus ist die Erzeugung analoger Signale, um die Pulse des ATLAS Kalorimeters nachzubilden. Als Signalquelle wurde eine handelsübliche Grafikkarte benutzt. Für die Programmierung der Pulssequenzen und zur Ansteuerung der Karte wurde ein Softwarepaket entwickelt. Die Umwandlung der Grafikkartensignale, entsprechend den Eingangsspezifikationen des Präprozessors, wurde auf einer eigens entworfenen Leiterplatine realisiert, die sowohl eine Spannungstransformation als auch eine Signalvervielfältigung durchführt. Eine zusätzliche Schaltung zur Synchronisierung der Signale mit der Abtastrate des Präprozessors wurde auf einer separaten Platine verwirklicht. Die Funktionstüchtigkeit des Testaufbaus wurde durch eine abschließende Messung demonstriert.

Abstract

Rate Metering is a valuable instrument to monitor the activity of the ATLAS calorimetry at trigger level. This thesis is concerned with the study of the expected rates and the development of a test setup for the Rate Metering and Histogramming functionality of the ATLAS Level-1 Calorimeter Trigger PreProcessor. Based on data from a full physics and detector simulation, the expected rates during operation of the experiment at the Level-1 Calorimeter Trigger input were analysed. Also, their dependence on energy thresholds was determined. The test setup comprises the generation of analogue signals in order to simulate the pulses of the ATLAS calorimeters by the use of a commercial graphics card as signal generator. A software package was developed to create pulse sequences and to control the graphics card's output. To adapt the output signal to the requirements of the PreProcessor input, transformation, fan-out of the signal were realised by the design of a printed circuit board. Furthermore, an additional auxiliar device was assembled to synchronise the signals with the sampling rate of the PreProcessor System. A final measurement showed that the setup is more than adequate to test the Rate Metering functionality.

Contents

Introduction

The Large Hadron Collider (LHC) at CERN, which starts operation in the second half of 2008, will extend the existing knowledge about fundamental physics to a new energy range, the so-called terascale. It will collide protons with a center-of-mass energy of 14 TeV at an interaction rate of 1 GHz to search for new physics effects and especially for the yet undiscovered Higgs boson, the last missing particle in the Standard Model of particle physics. Among the four main experiments that are located at the LHC to explore the emerging new physics, ATLAS is one of the two general purpose detectors. The analysis of the physics processes at the high interaction rate at the LHC is very challenging, since the cross section to produce a Higgs boson is several orders of magnitude below those of the dominating background processes. Therefore, an effective online preselection of the interesting events is mandatory, a task that is performed by the ATLAS Trigger System.

This thesis is concerned with the Rate Metering and Histogramming functionality of the PreProcessor Module, which is the very first stage of the ATLAS Level-1 Calorimeter Trigger. It is an instrument to survey the activity of the ATLAS calorimetry at a level that is unbiased from trigger decisions. Thus it is the only in-situ tool that has access to all event data before any information is discarded. In the early phase of the experiment, this will be used primarily for diagnostic purposes, while the mid-term and long-term tasks are calibration and maintenance of the system.

The Rate Metering counts the occurrences of input signals that exceed a programmable threshold for each channel of the PreProcessor. The result is a signal rate for each Trigger Tower of the Level-1 Calorimeter Trigger, which provides easily accessible information about dead or hot channels. Furthermore, it achieves high statistics and is therefore predestined for calibration purposes. The Histogramming functionality records the energy distribution in each channel of the Level-1 Calorimeter Trigger. This allows the examination of oddly behaving channels in more detail.

Currently, the experiment and its subsystems are in a commissioning phase. This also includes the PreProcessor Module and as part of it the Rate Metering. The development of a self-contained test setup for a thorough examination of the functionality of the Rate Metering and Histogramming is one of the main objectives of this thesis. Moreover, it is concerned with the simulation of the Rate Metering and Histogramming in order to gain information about the expected rates in the running experiment.

The first chapter is an outline of the Standard Model of particle physics with focus on the Higgs boson, and it furthermore explains the strategy for its discovery at proton-proton collisions. The experiment that is intended to search for the Higgs boson, the Large Hadron Collider and the ATLAS detector with its components, is introduced in chapter 2. The Trigger System of ATLAS is described in chapter 3 with particular interest on the Level-1

Calorimeter Trigger and its PreProcessor System. The fourth chapter is dedicated to the Rate Metering and Histogramming functionality of the PreProcessor Module. It gives a review of the hardware implementation and shows the dependency of rates on threshold energy, luminosity and the readout frequency. Based on this study, a set of reasonable configurations is presented exemplarily for the different purposes of Rate Metering. Chapter 5 is concerned with the setup that is required to test the Rate Metering hardware implementation. It was developed in the course of this thesis and comprises the generation of analogue signals in order to simulate the pulses of the ATLAS calorimeters by the use of commercial graphics cards as signal generator. After the presentation of the basic idea, it follows an overview of the software package that was written for that special purpose. Subsequently, a detailed description of the development and design of a printed circuit board and a soldered circuitry that are mandatory for signal transformation, fan-out and synchronisation purposes is given. The chapter concludes with measurements to prove the functionality of the test setup. Finally, the results of this work are summarised in chapter 6, including an outlook on future ideas and measurements.

Chapter 1

Physics at ATLAS

1.1 The Standard Model

The Standard Model (SM) is a theory that describes the properties and interactions of the fundamental particles in physics. A comprehensive description of the SM can be found in [1], whereas the following section will give a brief introduction only.

The particles in the Standard Model are classified in two types, namely fermions with half-integer spin, and bosons with spin 1. *Leptons* (ℓ) are of the first kind and exist in three flavours (also often referred to as *generations*): the electron e, the muon μ and the tau τ. Each flavour comprises a so-called weak doublet consisting of the just mentioned massive particle with charge -1 and a nearly massless neutrino with no charge. The other fermionic particles are the *quarks* (q). Due to their electric properties and masses, they can be grouped similarly into three generations with two particles each as summarised in table 1.1. Quarks carry so-called colour charge[1], which is subject of the strong interaction. Due to the nature of the strong force, they cannot be isolated, but are confined with other quarks to form the *hadrons*. The most prominent hadrons are the neutron and the proton, the constituents of the matter that surrounds us. It consists of quarks and leptons of the first generation. Besides, every particle has an antiparticle counterpart with same spin and mass, but opposite charge. The Standard Model comprises three kinds of interactions: strong, weak and electromagnetic interaction. The gravitation is not included since it is only considerable for large masses. The carriers of the forces between the fermions are the gauge bosons (table 1.2):

[1]The expression *colour charge* is used as an intuitive analogon to the visual colours to settle the association of three types of charge with the three colours red, green and blue (and their *anti*colours antired ($\overline{r}$), antigreen ($\overline{g}$) and antiblue ($\overline{b}$). Colours that combine to be colourless are charge neutral.

fermions	generation			interaction			
	I	II	III	em	weak	strong	grav.
quarks	u	c	t	✓	✓	✓	✓
	d	s	b	✓	✓	✓	✓
leptons	ν_e	ν_μ	ν_τ	-	✓	-	?
	e^-	μ^-	τ^-	✓	✓	-	✓

Table 1.1: Organisation of fermions in the Standard Model and their interactions.

interaction	gauge boson	couples to
strong	gluon g	colour charge
em	photon γ	electr. charge
weak	$W^{\pm}$ / Z^0	weak charge

Table 1.2: The mediators of interactions in the Standard Model.

Gluons (g) mediate the strong interaction by coupling to the colour charge. Since gluons carry a colour charge themselves there is a self-coupling which is unique among the gauge bosons. Holding a colour and an anticolour, eight types of gluons exist. The strong interaction is decribed by the theory of *quantum chromodynamics* (QCD).

Photons (γ) are the carriers of the electromagnetic force, they couple to the electric charge. The electromagnetic interaction is described by the theory of *quantum electrodynamics* (QED).

Vector bosons $W^{\pm}$ and Z^0 mediate the weak interaction. They are massive bosons and couple to all fermions.

The electromagnetic and the weak force are unified within the theory of the electroweak interaction.

The Standard Model has been developed almost 40 years ago and was confirmed by a considerable amount of experiments; all measurements could be explained within the framework of the Standard Model. Moreover, it describes the interaction of particles with tremendous accuracy and even allowed the prediction of new particles as the top quark and the $W^{\pm}$ / Z^0 bosons. However, it does not explain why the particles have certain properties – in fact, these are parameters that have to be determined with experiments and introduced into the theory. In addition, the Standard Model encounters some other problems like e.g the explanation for the difference of several orders of magnitude in the strength of the interactions, also known under the term *hierarchy problem*. There are approaches to extend the Standard Model in order to solve the hierarchy problem, like e.g. supersymmetry [2] and extra dimensions [3].

But, one of the most prominent open questions is how the mass is assigned to the particles.

1.1.1 The Higgs Mechanism

The proposed solution to the mass problem in the framework of the Standard Model is the introduction of a fourth field of interaction, the so-called Higgs field [4]. This field yields the generation of mass as a consequence of the spontaneous symmetry-breaking of the electroweak theory. It results in non-zero masses through mass coupling to the fermionic particles and also allows the gauge bosons $W^{\pm}$ and Z^0 having masses. A detailed description of this so-called Higgs Mechanism can be found in [1].

A direct consequence of the introduced field is the existence of a neutral scalar particle with spin 0, the Higgs boson H. The mass of this Higgs boson cannot be predicted theoretically. It is a free parameter in the Standard Model. However, a limit can be set from unitarity arguments ($m_{\mathrm{H}} <\sim 1\,\mathrm{TeV}$) and the mandatory stability of the electroweak vacuum ($m_{\mathrm{H}} > 80\,\mathrm{GeV}$).

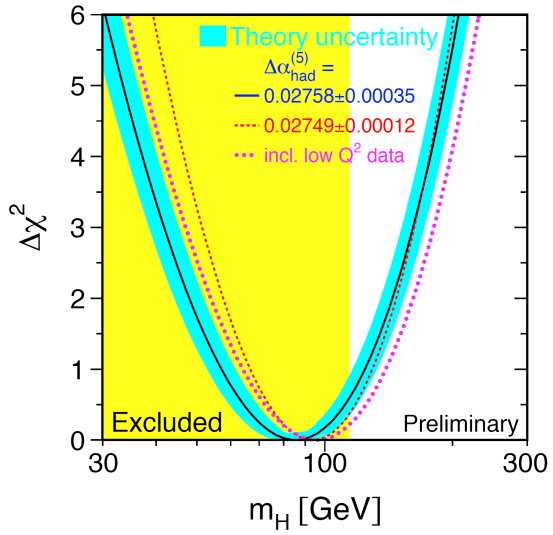


Figure 1.1: Estimation of the Higgs mass from a combinatorial fit of the measured parameters of the Standard Model, assuming that there is a Standard Model Higgs [5].

Furthermore, the combined results of former experiments imply the Higgs mass to be most probably in the minimum of the curve in figure 1.1, which shows the $\Delta\chi^2$ estimated by a global fit of the measured Standard Model parameters. Additionally, the direct search for the Higgs boson excluded a mass below $\sim 114\,\mathrm{GeV}$.

1.1.2 Higgs Decay Modes

decay channel	Higgs mass range [GeV]
$H \to b\bar{b}$	$90 < m_{\mathrm{Higgs}} < 130$
$H \to \gamma\gamma$	$80 < m_{\mathrm{Higgs}} < 160$
$H \to WW^{(*)} \to \ell\nu\ell\nu$ $H \to WW \to \ell\nu jj$	$150 < m_{\mathrm{Higgs}} < 190$
$H \to ZZ \to \ell\ell jj$ $H \to ZZ^{(*)} \to 4\ell$	$140 < m_{\mathrm{Higgs}} < 1\,000$

Table 1.3: Dominating Higgs decay modes. j denotes a so-called jet[2].

The Higgs boson is measured through its decay modes. Figure 1.2 shows the branching ratios of the Higgs for its main decay channels as a function of its mass. Since it couples to masses, branching ratios of decay channels including heavy particles dominate. In the region below 140 GeV, these are the decays to fermion anti-fermion pairs, whereas at higher masses, the decay modes to ZZ and to W^+W^- prevail. Since the mass of the Higgs cannot be predicted, the detector has to be optimised likewise on all decay modes over the full mass range. The most important decay modes are summarised in table 1.3.

[2] A jet is a narrow cone of hadronising quarks and gluons.
[3] For the definition of the luminosity, see formula 2.1.

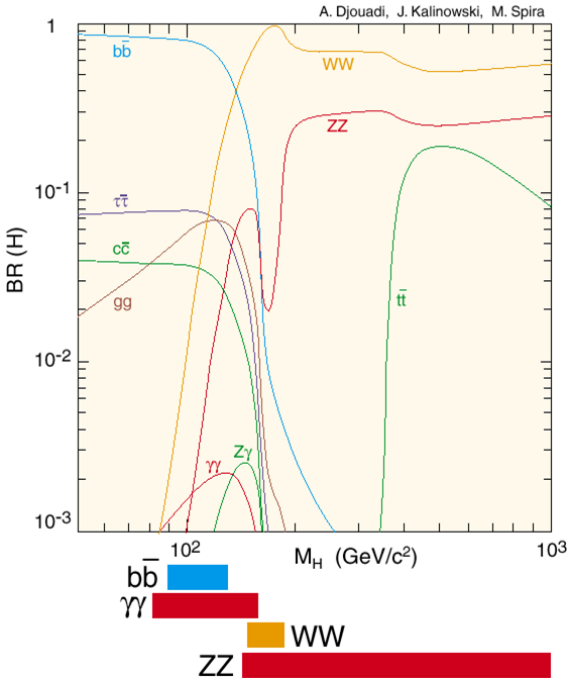


Figure 1.2: Branching ratios of the Higgs decay modes as a function of the Higgs mass. The bars below the plot indicate the most promising discovery channels.

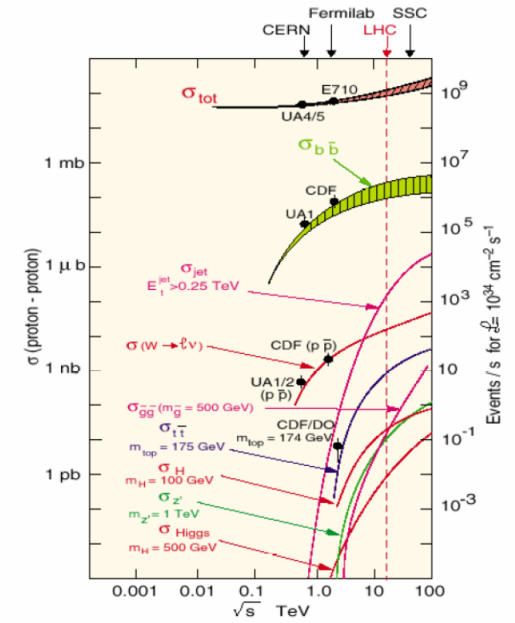


Figure 1.3: Cross section of the different processes in inelastic proton-proton collisions as a function of the center-of-mass energy for a instantaneous luminosity[3]of $\mathcal{L} = 10^{34}\,\frac{1}{\mathrm{cm}^2\mathrm{s}}$.

1.2 Requirements for the Experiment

The discovery of the Higgs boson is the main objective of the ATLAS experiment at the upcoming high energy at CERN, the Large Hadron Collider (LHC). The LHC will provide proton-proton collisions with a center-of-mass energy of $\sqrt{s} = 14\,\mathrm{TeV}$ in order to explore the so-called *terascale* of high energy physics. An introduction to the LHC and the ATLAS detector will be given in chapter 2, whereas the following sections focus on the requirements for the experiment as a whole.

Proton-Proton Physics

The proton is composed of three quarks as valence quarks (up, up, down), giving the proton its properties, and a sea of virtual quarks. Since the quarks are confined in the proton by the strong interaction, colliding protons mostly scatter elastically, i.e. the protons remain stable and are only deflected marginally as a whole at very small angles with respect to the beam axis. However, at very high energies, the distance of the partons eventually is short enough that they can be considered free within the range of the strong force ($10^{-15}\,\mathrm{m}$) and are able to interact. These processes are called inelastic or hard scattering and produce new particles in the limits of the Standard Model, with the Higgs boson being the most interesting one.
In order to cover the entire mass range in which the Higgs boson is expected, a center-

of-mass energy of $\sqrt{s} = 1\,\text{TeV}$ of the colliding partons is mandatory for the direct search. Unfortunately, the interacting partons in proton-proton collisions only hold a fraction x_1 and x_2 of the protons' total momentum. Hence, a center-of-mass energy of $\sqrt{s} = 14\,\text{TeV}$ is intended for the LHC to cover the full range of the possible Higgs mass.

Higgs Production

Figure 1.3 shows the partial cross sections of processes in proton-proton collisions as a function of the center-of-mass energy $\sqrt{s}$. It reveals that the hard scattering processes containing the interesting physics are very rare and only contribute marginally to the total inelastic cross section in proton-proton collisions. Concerning e.g. the direct production of a Higgs boson with a mass of $m_{\text{Higgs}} = 500\,\text{GeV}$, this means that only one event out of 100 000 000 000 includes a Higgs boson. As a consequence, an experiment that wants to discover the Higgs has to achieve not only a very high center-of-mass energy, but also tremendous statistics in order to produce a significant amount of the particles of interest.
It is obvious that this puts also stringent requirements on the detector, since it has to provide a sufficient resolution to be able to separate the particles from the overlapping events and also a minimal dead time in order to cope with the extraordinary high interaction rate. Moreover, it must be able to search in all possible Higgs decay modes equally since the mass of the Higgs cannot be predicted. Also, the event selection is a similarly demanding task, in which the very rare processes of interest have to be identified and selected for a permanent storage, whereas the by far larger amount has to be discarded since it would be impossible to save all data to disc.

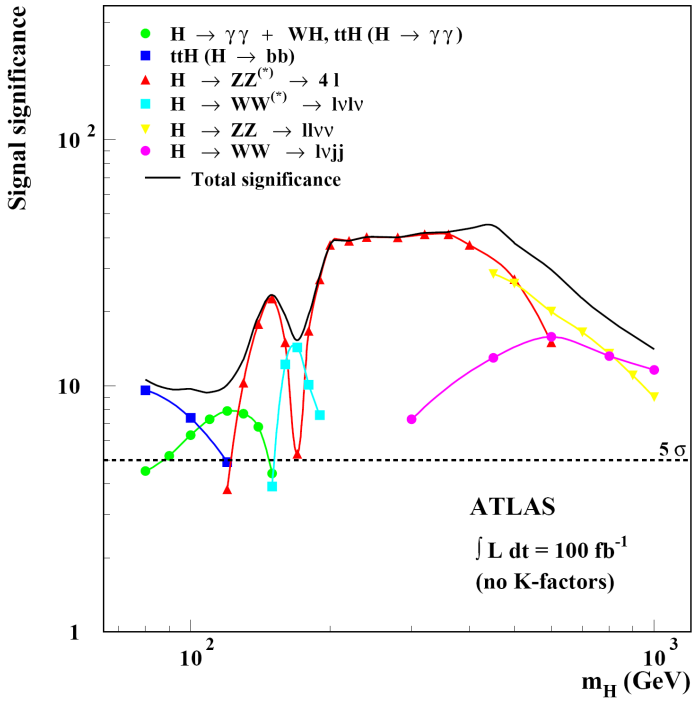


Figure 1.4: Discovery potential of the Higgs boson at the ATLAS experiment after one year of operation at the design luminosity of the LHC as a function of its mass. The 5σ discovery line is shown as dotted line [6].

The ATLAS experiment, introduced in the next chapter, is designed for the detection of the Higgs boson in all decay channels. Figure 1.4 shows the discovery potential of the Higgs boson at the ATLAS experiment for every channel individually as well as the total discovery potential. With the LHC operating at the design luminosity $\mathcal{L} = 10^{34}\,\frac{1}{\mathrm{cm}^2\mathrm{s}}$ (see section 2.1), the Higgs can be found with a signal significance of more than 5σ over the entire mass range from 80 GeV to 1 TeV after one year of operation.

Chapter 2

The ATLAS Experiment at the Large Hadron Collider

2.1 The Large Hadron Collider

The *Large Hadron Collider* (LHC) at the European Organization for Nuclear Research (CERN) in Geneva is currently nearing its completion and will start operation in the second half of 2008. It will reach higher energies than all particle accelerators ever built before and thus open a new chapter of research in particle physics. Designed to collide two counter rotating beams of protons in a first phase and heavy ions at a later stage, it will achieve a center-of-mass energy of 14 TeV and 11 TeV per nucleon pair respectively.

Four main experiments are being installed at the LHC:

- ATLAS[1] and CMS[2] are multi-purpose discovery detectors to exploit the full range of physics available in proton-proton collisions at the LHC.
- ALICE[3] will examine heavy ion physics in the collision of lead ions.
- LHCb[4] is designed to observe rare decays of b quarks and to investigate CP[5] violation.

The LHC is hosted about 100 m below the surface in the former LEP[6] ring tunnel with a circumference of 27 km. Utilising existing structure available at CERN, the pre-accelerated particles are injected into the LHC ring with energies of 450 GeV. They are then further accelerated by a radio frequency system using superconducting cavities to the final center-of-mass energy. In contrast to the electron-positron accelerator LEP, where synchrotron radiation set the limiting factor for the center-of-mass energy, the limiting factor for the proton-proton and heavy ion collisions is mainly the maximum magnetic field that can be produced by the bending magnets for the particle beams. A tremendous technical effort is needed to generate extraordinary high magnetic fields. By cooling the entire beam system to 1.9 K using helium in a superfluid state, magnetic fields of up to 8.33 T are achieved. In total,

[1] ATLAS - **A** **T**oroidal **L**HC **A**pparatu**S**
[2] CMS - **C**ompact **M**uon **S**olenoid
[3] ALICE - **A** **L**arge **I**on **C**ollider **E**xperiment
[4] LHCb - **L**arge **H**adron **C**ollider **b**eauty
[5] CP - **C**harge and **P**arity conjugation
[6] LEP - **L**arge **E**lectron **P**ositron Collider

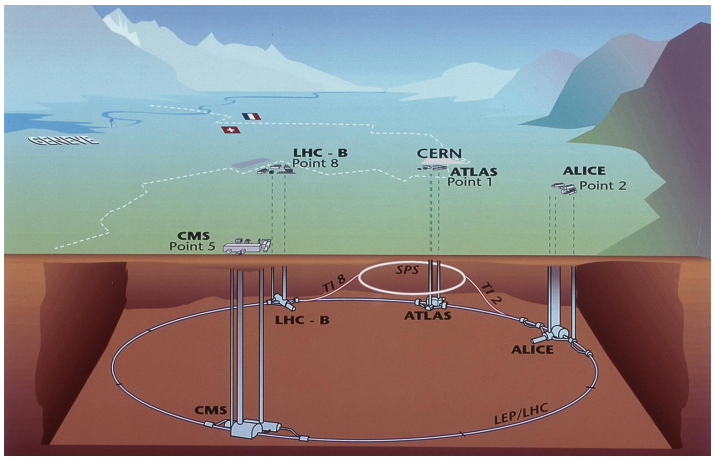


Figure 2.1: Sketch of the Large Hadron Collider with its four main experiments [7].

1232 superconductive dipole magnets are installed throughout the eight bending octants of the collider ring, complemented by another 386 quadrupole magnets for beam focusing and several thousand of additional correction magnets. Since the colliding particles at the LHC have the same charge, the accelerator consists of two vacuum pipes each equipped with dipole magnets in opposite direction, which are kept in a two-in-one magnet cryostat for compactness.

Since the cross section for deep inelastic scattering events that contain the interesting physics like e.g. the Higgs production is expected to be very small (see section 1.3), a high interaction rate is mandatory to acquire sufficient statistics. The respective parameter that expresses the performance of the accelerator is the *instantaneous luminosity* $\mathcal{L}_{\text{inst}}$, giving the number of particles per area and time at the interaction point. For a circular accelerator, it is given by the formula

$$\mathcal{L}_{\text{inst}} = \frac{N_{\text{a}} \cdot N_{\text{b}} \cdot j \cdot v/C}{A}, \tag{2.1}$$

where N_{a} and N_{b} are the numbers of protons in the interacting bunches a and b, j is the number of bunches in the beam, v is the velocity of the protons, C is the circumference of the accelerator ring and A is the cross section area at the interaction point. The interaction cross section σ and the luminosity $\mathcal{L}$ give the total reaction rate R:

$$R = \sigma \cdot \mathcal{L}_{\text{inst}}$$

The protons at the LHC are organised in bunches of 10^{11} particles with a length of 7.55 cm in beam direction, a maximum diameter of 16.7 µm and a spacing of 7.5 m between the bunches. In total, 2808 bunches are contained in the LHC ring at operation[7], leading to a design luminosity of $\mathcal{L}_{\text{inst}} = 10^{34}\,\frac{1}{\text{cm}^2\text{s}}$ and an average amount of 23 inelastic proton-proton interactions per *bunch crossing* (BC) occurring every 24.95 ns.

2.2 The ATLAS Detector

ATLAS is a general purpose detector, designed for comprehensive studies of the physics within the LHC's energy range. The main objective is the search for the Higgs boson in a wide mass

[7]In principle, 3564 bunch places are available in the ring, but for technical reasons during the filling process and because of the gap that is needed for a controlled beam dumping, only 2808 slots are occupied.

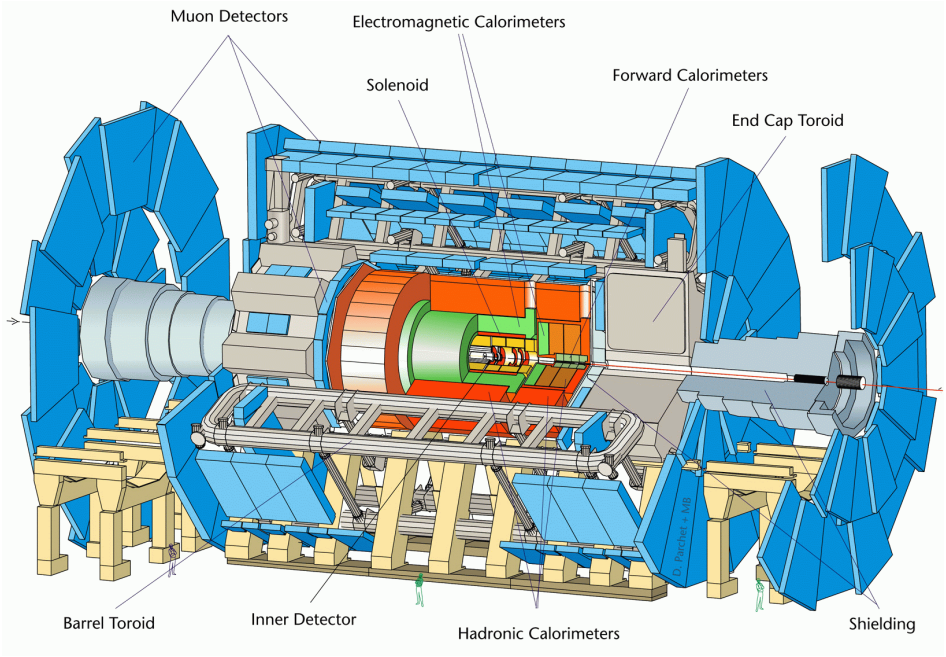


Figure 2.2: The ATLAS detector. It consists of the Inner Detector in the very center (yellow), the calorimetry surrounding it (green and red) and the large muon spectrometer in the outer region (blue) [6].

range (see section 1.1.1), but also to measure fundamental parameters of the Standard Model with unprecedented accuracy, e.g. the masses of the $W^{\pm}$ bosons as well as the mass of the top quark. Since the LHC will reach unrivalled energy ranges, ATLAS will moreover probe new physics beyond the Standard Model like possible substructure of the fundamental particles (compositeness), supersymmetric particles or the existence of extra dimensions and micro black holes.

The design, construction and operation of ATLAS involve the largest collaboration effort that was ever carried out in the history of physical science. 2 100 physicists and engineers from 37 countries and 167 universities are contributing to the success of ATLAS. The detector is currently in the commissioning phase and will start operation with the first beam at the LHC.

The comprehensive exploration of the variety of physics accessible in proton-proton collisions at the LHC requires a detector with the following basic criteria:

- An **excellent electromagnetic and hadronic calorimetry** with full coverage of the solid angle is needed for a precise identification and measurement of electrons and photons on the one hand and the hadronic jets on the other hand as well as the estimation of missing transverse energy.

- A **very accurate muon spectrometer** is required for the identification of muons and the precise measurement of their momenta.

- A **tracking system with very high granularity and strong magnetic field** has to be provided in order to resolve tracks of high-p_{T} leptons and to identify electrons, photons, τ-leptons at highest luminosities.

- An **efficient trigger system** is needed to select the events of interest that are very rare compared to the dominating QCD background.
- In general, a **very high granularity** of all components of the detector is mandatory in order to resolve particles at the highest luminosities with multiple overlapping events, as well as a **large acceptance** in the solid angles and an **exceptional radiation hardness**.

Figure 2.2 shows the ATLAS detector layout. It comprises the *Inner Detector* in the very center, the calorimetry surrounding it and the muon spectrometer in the outer region. In total, ATLAS has a length of about 45 meters, a height of more than 25 meters, and weighs about 7 000 tons.

The Coordinate System

The beam direction defines the z-axis of the ATLAS coordinate system, with the positive z pointing towards the LHCb experiment (see figure 2.1). This side of the detector is called the *side-C*, and the negative z is the *side-A*. The x-y plane is transverse to the beam axis. The x-axis points to the center of the LHC ring, and the y-axis points upwards. The azimuthal angle ϕ is measured around the beam axis, whereas the polar angle θ relates to the angle from the beam axis. The *pseudorapidity*[8] η is defined as $\eta = -\ln\tan\theta/2$. It is introduced because differences $\Delta\eta$ are invariant under the Lorentz transformation. R finally denotes the radial distance in pseudorapidity-azimuthal angle space.

2.2.1 The Magnet System

The magnet configuration is composed of two systems with different magnetic field orientation. The tracking system in the inner detector cavity is surrounded by a thin solenoid magnet that provides a homogeneous magnetic field of 2 T parallel to the beam axis. It uses the absorber material of the hadronic calorimeter as its return yoke. For the muon spectrometer, ATLAS uses a large air-core toroid system producing a magnetic field circular around the beam axis. It consists of eight independent coils arranged around the hadronic calorimeter for both the barrel and the two end-caps. With a length of 25 m and a width of 5 m, the toroid magnets define the considerable overall size of the ATLAS detector.

2.2.2 The Inner Detector

At the design luminosity of the LHC, approximately 1 000 particles are produced in every bunch crossing merely within $|\eta| < 2.5$. The *Inner Detector*'s objective is the reconstruction of tracks of these particles and the determination of the vertices of the primary interactions and eventual secondary vertices. This requires a tracking system with a very high granularity to resolve the tracks of multiple overlapping events, a short dead time in order to minimize pile-up effects, an accurate momentum resolution and a considerable radiation hardness due to its proximity to the interaction point.
Figure 2.3 shows the layout consisting of the high-resolution semiconductor *Pixel Detectors* in the very center, surrounded by a two-part *Semiconductor Tracker* (SCT) for the barrel

[8] The rapidity y is defined as $y = \frac{1}{2}\frac{E+p\cdot\cos\theta}{E-p\cdot\cos\theta}$. For $\beta \to 1$, the rapidity becomes $\lim_{\beta\to 1} y = -\ln\tan\theta/2 = \eta$.

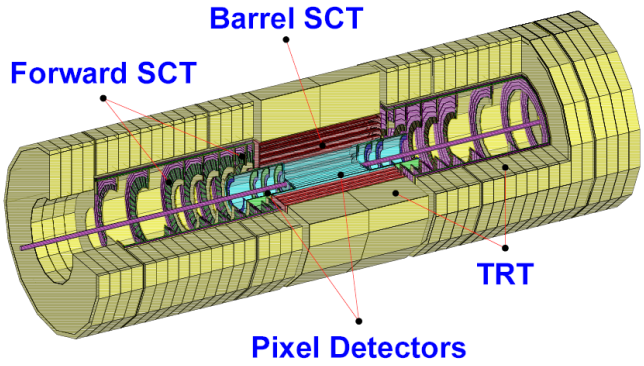


Figure 2.3: Layout of the Inner Detector [8].

and the forward region, and a similarly divided *Transition Radiation Tracker* (TRT) to cover the wide ranging outer region. The Inner Detector provides a continuous coverage in ϕ and an acceptance in η from -2.5 to 2.5, amounting to a size of 7 m in length and a diameter of 2.3 m of the cavity. In order to measure the momenta of the particles, the solenoid magnet field penetrates the whole cavity in beam direction.

The semiconductor Pixel Detector consists of three barrels staggered in transverse direction to the beam and five discs on either side. It uses silicon pixel technology with an average density of 50 pixels per mm^2 and an intrinsic accuracy for measuring the space points of 10 µm in R-ϕ and 115 µm in z-direction for the barrels and also 115 µm in R for the discs respective. The total amount of readout channels is about 80.4 million.

The Semiconductor Tracker (SCT) consists of silicon microstrip detectors in four layers for both the barrel and the end-cap region. Each layer is composed by two sets of strips with perpendicular orientation in order to measure the space point of the crossing particles. The strips have a length of 6.4 cm and a pitch of 80 µm and achieve a measuring accuracy of 17 µm (R-ϕ) and 580 µm (z in the barrel and R in the discs). In total, the SCT comprises 6.3 million readout channels on an area of 61 m^2.

The Transition Radiation Tracker (TRT) uses a large number of straw tubes with a diameter of 4 mm and a length of up to 144 cm. Typically, single particles are detected by about 36 straws per track, each with an intrinsic accuracy of 130 µm. Overall, about 350 000 straw tubes are assembled in the TRT.

2.2.3 The Calorimeters

The ATLAS calorimetry is dedicated to the energy measurement and the identification of isolated leptons, photons and hadrons, jets and the estimation of the missing transverse energy[9] $E_{\mathrm{T}}^{\mathrm{miss}}$. The calorimeter system is composed of two parts: the *Electromagnetic Calorimeter* (EM) and the *Hadronic Calorimeter* (HAD). Both are furthermore divided into several sections along the pseudorapidity η. The central region is referred to as the *barrel* covering a range of $|\eta| < 1.475$ for the EM and $|\eta| < 1.7$ for the HAD respectively. The so-called *end-caps* reach until $|\eta| = 3.2$ for both calorimeters. The very forward region for $|\eta| < 4.9$

[9] E_{T} is defined as $E_{\mathrm{T}} = E \cdot \cos\theta$.

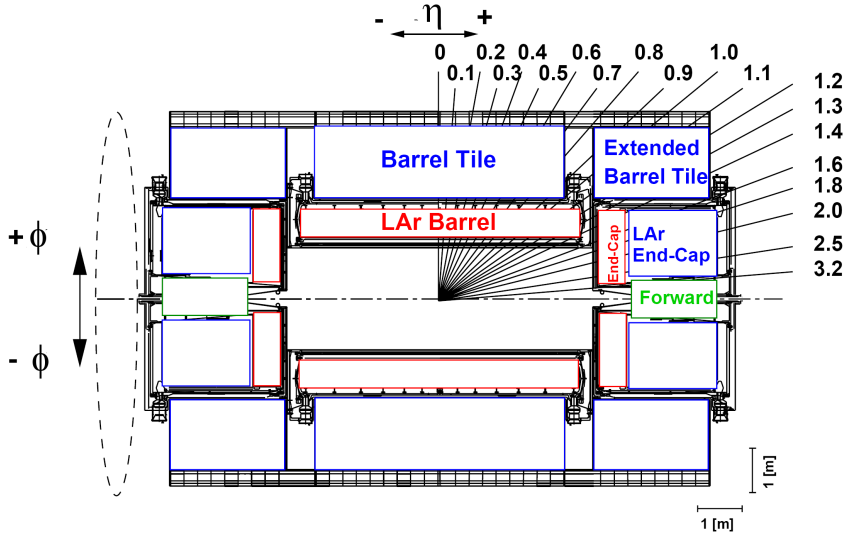


Figure 2.4: Overview of the ATLAS calorimetry [9].

is covered by the forward calorimeter (FCAL), which is a two-part system attributed to the hadronic calorimeter. Figure 2.4 shows the layout of the ATLAS calorimetry.
Two basic types of sampling calorimeters are utilised in the ATLAS calorimeter system. Liquid-Argon (LAr) technology in combination with several absorber materials is used for the electromagnetic calorimeter and the end-cap and forward region of the hadronic calorimeter. The barrel of the hadronic calorimeter in contrast is built of layers of iron and scintillator since it is the return yoke of the solenoid magnet of the inner detector. The principle for both is the same, consisting of a layer structure of alternating passive and active material: the primary particles interact dominantly with the absorber material and provoke a cascade of secondary particles, while the resulting particle showers are detected by sensitive layers behind it. The underlying processes in contrast are completely different for electromagnetic and hadronic particles. While for electrons and photons Bremsstrahlung and pair production are the main processes, intranuclear processes from inelastic interactions with the absorber material dominate in the case of hadrons. A good containment for the electromagnetic and hadronic showers is mandatory for the calorimetry. The total spatial depth of the EM exceeds 22 radiation lengths[10] X_0 in the barrel and 24 X_0 in the end-caps, so that electrons and photons deposit their energy almost completely in the electromagnetic calorimeter. Hadrons also loose a considerable amount of energy in the electromagnetic calorimeter already, but they penetrate deeper into the calorimetry. The depth of the calorimetry at $\eta = 0$ amounts to 2.3 interaction lengths λ from the EM, 7.4 λ from the HAD and 1.3 λ from the outer support, so that the total interaction length is 11 λ, which can be considered sufficient to prevent considerable punch-throughs into the muon system.

The energy resolution of a sampling calorimeter can be parametrised as follows:

$$\frac{\Delta E}{E} = \frac{a}{\sqrt{E}} \oplus \frac{b}{E} \oplus c,$$

where E is the energy, a is the sampling term, b the noise term and c the constant term. The

[10] The radiation length X_0 is the distance over which the energy of the electron is reduced by a factor $1/e$

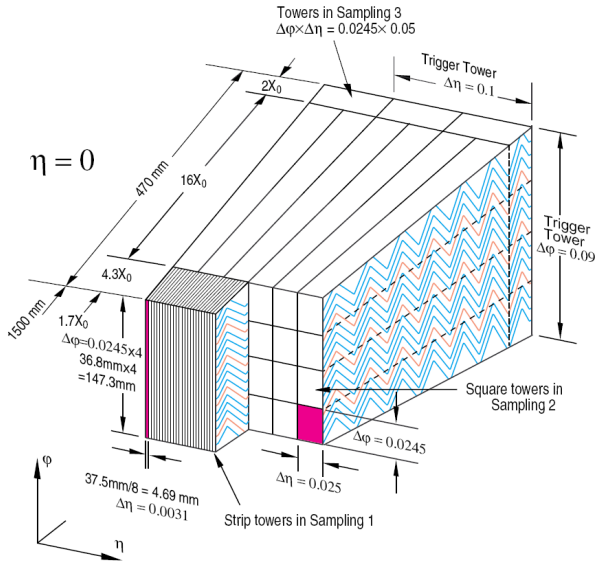


Figure 2.5: Layout of the accordion structure of the electromagnetic calorimeter. The passive and active material alternate, and the accordion structure guarantees a complete coverage in ϕ [10].

parameter a takes into account the geometrical shape of the calorimeter and the statistical shower development. Therefore, the sampling term is proportional to $1/\sqrt{E}$. b is the noise contribution to the energy measurement. Since the noise is independent from the measured energy of the incident particle, it is negligible for high energies. The constant term c comprises calorimeter parameters like resolution, calibration etc. and dominates for high energies.

The Electromagnetic Calorimeter

Figure 2.5 shows the layout of the electromagnetic calorimeter, which is also called accordion calorimeter because of the characteristic geometry. The advantage of the bent shape is the total coverage of the azimuthal angle without any cracks.
In radial distance to the interaction point, the electromagnetic calorimeter is segmented in three so-called *samplings*. The first has a depth of $4.3\,X_0$ and is composed of *strip towers* for a high granularity of 0.0031 in η, while being coarser in the azimuthal angle, $\Delta\phi = 0.098$. Sampling 2 has a granularity of 0.025×0.0245 in $\Delta\eta \times \Delta\phi$ and constitutes the biggest part of the accordion calorimeter with $16\,\mathrm{X}_0$. The thin third sampling ($2\,X_0$) in the outer region is again slighter coarser in η with 0.05×0.0245 in $\Delta\eta \times \Delta\phi$. Altogether, the accordion calorimeter holds 190 000 channels.
It uses lead plates as absorber material, because it has a high cross section for Bremsstrahlung and pair production, and LAr for the sensitive layers. A copper electrode is placed in between the two layers for the readout of the ionisation initiated by crossing charged particles. The thickness of the sensitive layer on each side of the electrode is 2.1 mm, which results in a drift time of about 450 ns for an operating voltage of 2000 V. The expected energy resolution of the electromagnetic calorimeter is

$$\sigma_E/E = 10\%/\sqrt{E} \oplus 3\%.$$

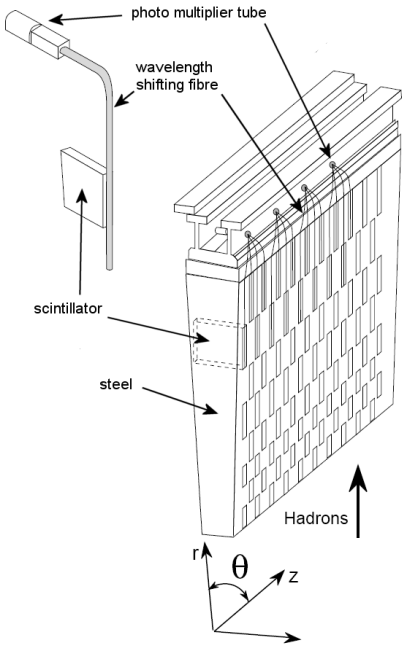


Figure 2.6: Sketch of a single tile calorimeter module. It consists of iron as absorber material and scintillating tiles, which are read out by photo multiplier tubes via wavelength shifting fibers [11].

The Tile Hadronic Calorimeter

The Tile Hadronic Calorimeter (TileCal) uses iron as absorber and scintillation tiles as active material. Figure 2.6 shows the layout of a TileCal segment. The self-supporting structure is designed to provide almost seamless coverage of the azimuthal angle. The tiles have a thickness of 3mm and are placed in parallel to the particle direction. The two open sides of the tiles are read out via wavelength shifting fibers, which transmit the emitted light to two photo multiplier tubes installed on top of the modules.

The TileCal is composed of two parts, the barrel tile for $|\eta| < 1.0$ and the extended barrel tile for $0.8 < |\eta| < 1.6$ (see figure 2.4), consisting of three layers each. The corresponding interaction length is 1.5, 4.1 and $1.8\,\lambda$ for the barrel and 1.5, 2.6 and $3.3\,\lambda$ for the extended barrel. The granularity of the TileCal is mostly 0.1×0.1 in $\Delta\eta \times \Delta\phi$, i.e. 64 segments in ϕ, adding up to about 10 000 channels. The energy resolution is aimed at

$$\sigma_E/E = 50\%/\sqrt{E} \oplus 3\%.$$

The Liquid Argon Hadronic Calorimeter and the Forward Calorimeter

The *Hadronic End-cap Calorimeter* (HEC) and also the *Forward Calorimeter* (FCAL) again use LAr as sensitive material, whereas for the absorbing material copper (HEC) and tungsten (FCAL) are used because of the better resistance against radiation.
The performance goal for the energy resolution of the HEC is $\sigma_E/E = 50\%/\sqrt{E} \oplus 3\%$ and $\sigma_E/E = 100\%/\sqrt{E} \oplus 10\%$ for the FCAL respectively.

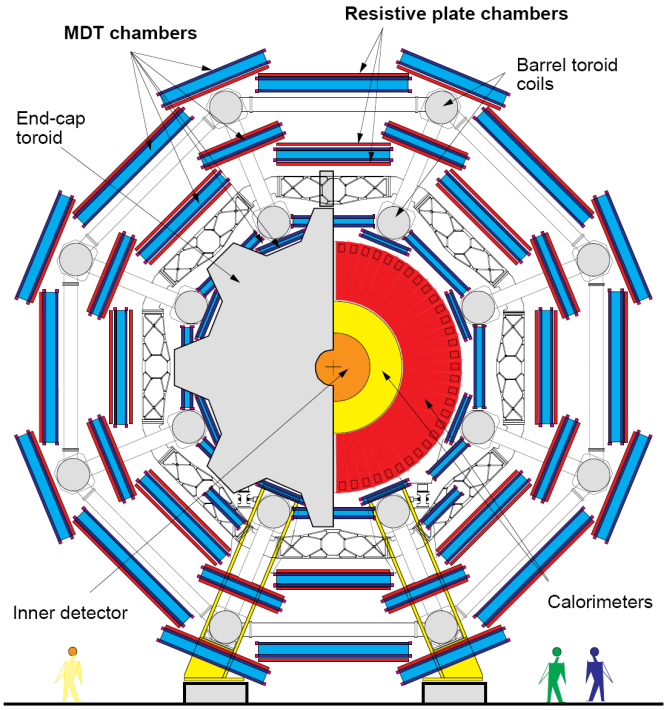


Figure 2.7: Cross-sectional view of the ATLAS detector. The muon spectrometer and its subsystems cover the entire outer part of the detector [12].

2.2.4 The Muon System

In contrast to electrons, photons, taus and jets, which are stopped within the calorimetry of ATLAS, muons traverse the calorimetry almost without interaction, being minimum ionising particles. Since high-momentum final-state muons are very promising and robust signatures for physics analysis, much effort was put in the muon system of ATLAS. Figure 2.7 shows the cross-sectional view of the central barrel of the ATLAS detector. Three layers are implemented to measure the deflection of muons in the magnetic field in order to determine their transverse momentum. The overall accuracy for the estimation of muons with a p_{T} of 1 TeV is planned to be $\sigma_{p_{\mathrm{T}}}/p_{\mathrm{T}} = 10\%$.
Four different types of gaseous tracking chambers are used in the muon system:

Monitored Drift Tubes (MDTs) modules consist of about 300 aluminium tubes with a diameter of 30 mm and a 50 µm thick wire along its central axis, obtaining a resolution of 80 µm per tube. 1 150 MDT modules are used in the barrel part of the muon system, amounting to a total number of 354 000 channels.

Cathode Strip Chambers (CSCs) are used in the first layer of the muon end-cap system since they provide a higher granularity and therefore are more adequate for the demanding rate and background conditions in the forward region. The CSCs are multi-wire proportional chambers with a cathode strip readout. In total, the CSC system comprises 31 000 channels.

Resistive Plate Chambers (RPCs) and **Thin Gap Chambers (TGCs)** are used for trigger purposes. The RPCs are composed of two parallel resistive plates with a narrow

component		required resolution	# channels	η coverage	
				measurement	trigger
tracking		$\sigma_{p_\mathrm{T}}/p_\mathrm{T} = 0.05\% p_\mathrm{T} \oplus 1\%$	87 000 000	± 2.5	-
EM		$\sigma_E/E = 10\%/\sqrt{E} \oplus 3\%$	190 000	± 3.2	± 2.5
HAD	barrel	$\sigma_E/E = 50\%/\sqrt{E} \oplus 3\%$	10 000	± 3.2	
	end-cap	$\sigma_E/E = 50\%/\sqrt{E} \oplus 3\%$	11 264	± 3.2	
	forward	$\sigma_E/E = 100\%/\sqrt{E} \oplus 10\%$	3 524	$3.1 < \lvert\eta\rvert < 4.9$	
muon spectrometer		$\sigma_{p_\mathrm{T}}/p_\mathrm{T} = 10\%$ at $p_\mathrm{T} = 1\,\mathrm{TeV}$	1 076 000	± 2.7	± 2.4

Table 2.1: General performance goals of the ATLAS detector [13].

gas gap in between, whereas the TGCs are designed similarly to the multiwire proportional chambers. Having a lower granularity in the order of centimeters, but a very fast response time of about 1 ns, they are suitable to cover a large area as trigger chamber. Both systems comprise 691 000 channels.

Since the muon system covers a very large area, an optical system consisting of 12 000 sensors continuously monitors the alignment of the detector components to guarantee the required precision for the momentum measurement.

2.2.5 Summary

The ATLAS detector is very well prepared to explore the full range of physics available at the LHC. Due to its high granularity in every subsystem of the detector, it resolves the enormous density of particles. The large acceptance in η and the almost full azimuthal angle coverage guarantee an exhaustive detection of particles and a good estimation of missing transverse energy $E_\mathrm{T}^\mathrm{miss}$. The tracking system achieves a very good charged-particle momentum resolution and vertex detection. The calorimeters provide an excellent energy resolution in both the electromagnetic and the hadronic subsystems. Likewise the muon spectrometer achieves a good muon identification and momentum resolution. Table 2.1 summarises the properties of the detector's subsystems in terms of resolution and the number of channels as well as the acceptance along the pseudorapidity η.

Chapter 3

The ATLAS Trigger System

At the LHC design luminosity of $\mathcal{L}_{\text{inst}} = 10^{34}\,\frac{1}{\text{cm}^2\text{s}}$, 23 overlapping events occur every 25 ns. This is a great challenge for the ATLAS Trigger and Data Acquisition System. Since only a tiny fraction of the events can be stored permanently, an effective and reliable in-situ event selection is required in order to single out the very rare events from the dominating QCD background. The total reduction factor that has to be achieved is given by the bunch crossing frequency of 40 MHz on the one hand and the data size of a complete detector readout on the other. Since the ATLAS detector comprises about 90 million channels from pixel detector, tracker, calorimetry and muon spectrometers altogether, the event size is considerable: Although a data reduction is included for the readout by e.g. omitting channels that contain only noise, the size per readout amounts to 1.5 MByte, resulting in the tremendous data rate of $\sim$ 60 TByte/s. Assuming a maximum of $\sim$ 300 MByte/s for the rate at which data can be stored to disc, the required data reduction is of the order of $\sim 2 \cdot 10^5$ and the event rate amounts to 200 Hz.

3.1 The Trigger Concept

In order to process the enormous quantity of data, a three level trigger system was proposed for ATLAS: the hardware-based Level-1 Trigger (L1), the software-based Level-2 Trigger (L2) and the Event Filter (EF). Figure 3.1 is a scheme of the trigger and data acquisition system. The Level-1 Trigger performs the first step in the selection of events. Its decision is based on data from the calorimeters with reduced granularity on the one hand and data from the trigger RPC and TGC of the muon spectrometer on the other. No data from the inner detector is used. The Level-1 trigger decision is based not on the topology of an event, but exclusively on the multiplicity (i.e. the number) of physics object candidates. However, the topology information is provided to the Level-2 Trigger as so-called *Region-of-Interest* (RoI). The L1 is a synchronous system with a fixed *trigger latency*[1], i.e. the events are continuously processed at a constant rate of 40 MHz and in a fixed time interval. In order to extend the available time for the trigger decision beyond the 25 ns between the interactions, the full event data is buffered in so-called pipeline memories. They have a length of 100 bunch crossings, which corresponds to $t = 2.5\,\mu$s and thus defines the absolute limit for the L1 trigger decision[2],

[1] The trigger latency is the time interval that the trigger needs to reach a decision.

[2] Since the limit must not be exceeded, the L1 was designed for a nominal latency of $t = 2.0\,\mu$s.

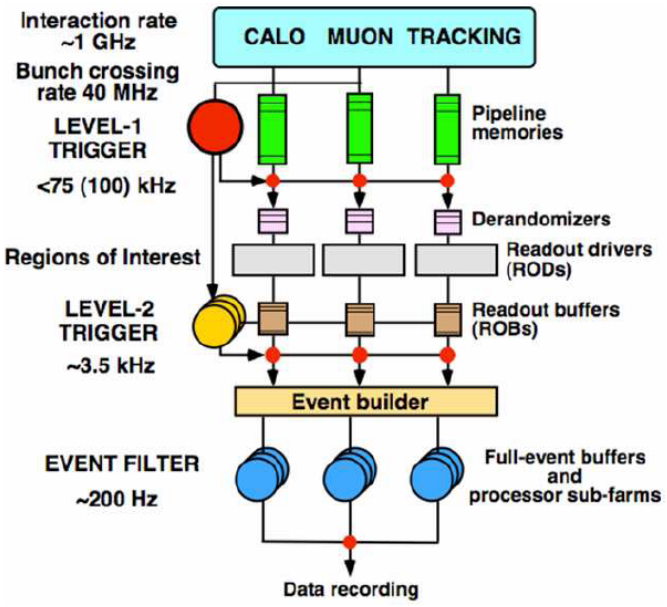


Figure 3.1: Scheme of the ATLAS trigger and Data Acquisition System [14].

including signal propagation within cables. For this demanding limit on the trigger latency and the high data rate, the L1 consists of custom-built pipelined parallel electronics with hard-wired algorithms implemented in ASICs[3] and FPGAs[4]. It achieves a reduction of the event rate of a factor of > 400, which corresponds to 100 kHz. The accepted events are passed to the Read-Out Buffers (ROBs) where they are stored during the Level-2 decision making. The Level-2 Trigger has access to all detector components, but only investigates a subset ($\sim$ 2% of the total readout data), which is defined by the RoIs provided by the Level-1 Trigger in parallel to the accepted events. The Level-2 Trigger consists of a large network of about 500 commercial CPUs linked by a high-capacity switched network. It is an asynchronous system, in which the incoming events are processed in parallel with varying processing time depending on the complexity of the event topology. The average processing time is 40 ms and the event rate is reduced to approximately 3.5 kHz.
Finally, the events that pass the Level-2 Trigger are fully reconstructed in the Event Filter. It is again an asynchronous system consisting of about 1 600 computers. Using similar algorithms as for the offline analysis, the event rate is reduced to the requested $\sim$ 300 MByte/s and the remaining event data is permanently stored.

3.1.1 Level-1 Trigger

The Level-1 Trigger comprises the *Calorimeter Trigger subsystem* (L1Calo), the *Muon Trigger subsystem* and the *Central Trigger Processor* (CTP). A scheme of the Level-1 Trigger System is shown in figure 3.2.
The decision making is based on the identification of various physics object candidates: isolated electrons and photons, taus, jets and muons. Furthermore the missing transverse energy

[3]ASIC - application-specific integrated circuit.
[4]FPGA - field-programmable gate array.

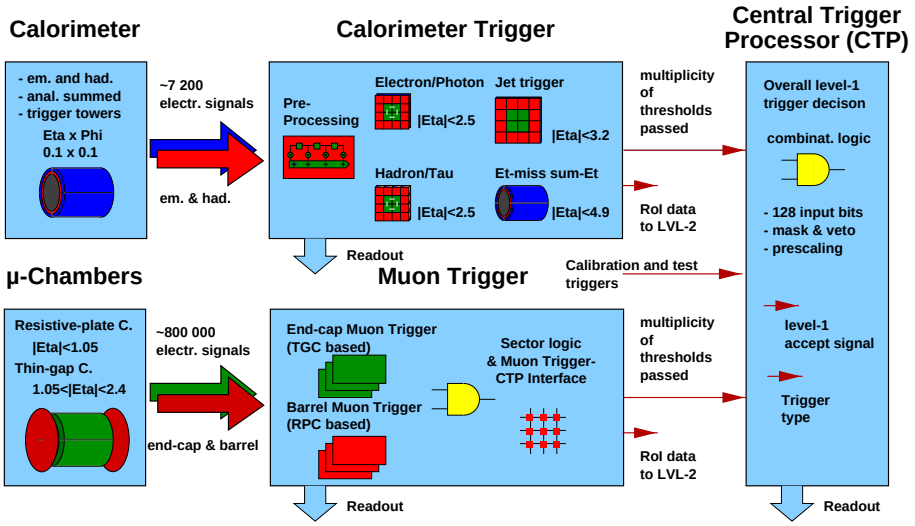


Figure 3.2: Scheme of the Level-1 Trigger System: Calorimeter Trigger, Muon Trigger and the Central Trigger Processor [9].

$E_{\mathrm{T}}^{\mathrm{miss}}$ is estimated from the total energy deposit $\sum E_{\mathrm{T}}$ in the calorimeter, since it is associated with nearly non-interacting particles as neutrinos. Those are of special interest i.e. in the Higgs decay channel $\mathrm{H} \rightarrow \mathrm{WW} \rightarrow \ell\nu jj$ and for physics scenarios beyond the Standard Model. The Level-1 Calorimeter Trigger makes its decision based on the energy depositions in the calorimeter system of ATLAS, more precisely the transverse vectorial component E_{T}. Performing several algorithms that evaluate the local energy distribution and compare it with programmable thresholds, the Level-1 calorimeter trigger passes the multiplicity of trigger object candidates to the CTP. It is important to mention that the Level-1 Trigger does not make use of the topology of an event itself. Rather the CTP holds a definition of multiplicity thresholds, the so-called *trigger menu*, which finally decides on keeping an event or not. In case of a positive trigger decision, the CTP sends a so-called *Level-1 Accept* (L1A) to the pipeline memories and the L1Calo subsystems in order to enable the data transmission of that particular event and all related information like e.g. the RoIs to the Level-2 Trigger. The architecture and algorithms are described in detail in chapter 3.2. The Muon Trigger decision relies on the reconstruction of muon path candidates from the 800 000 channels of the RPC and TGC trigger chambers (see section 2.2.4). It analyses the hits in different layers of the muon spectrometers in terms of spatial coincidences. The multiplicity of the track candidates is transmitted to the Central Trigger Processor, and in case of a L1A, the RoIs (i.e. the coordinates of the track candidates) are sent to the Level-2 Trigger.

3.2 The Level-1 Calorimeter Trigger

Figure 3.3 shows the scheme of the Level-1 Calorimeter Trigger. Its main building blocks are the *PreProcessor* (PPr), the *Cluster Processor* (CP) and the *Jet/Energy Processor* (JEP). The CP and JEP have so-called *Common Merging Modules* (CMM) attached. The *Read-Out Driver* modules (ROD) are responsible for the data acquisition of the system and provide the

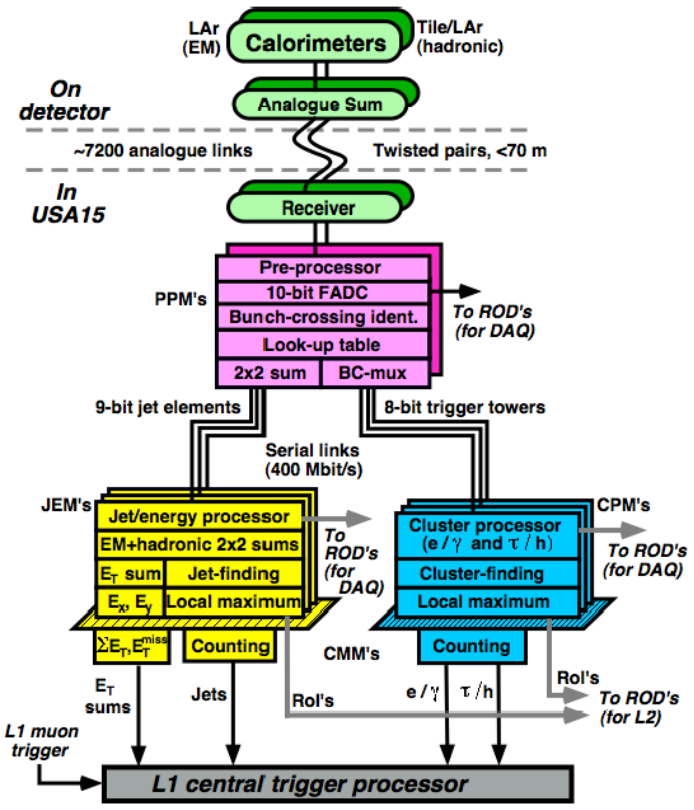


Figure 3.3: Architecture of the Level-1 Calorimeter Trigger [14].

RoIs to the Level-2 Trigger. The L1Calo system has a fixed latency, achieved by a pipelined digital system that processes the event data in parallel. It receives data at reduced granularity of 0.1×0.1 for $\Delta\eta \times \Delta\phi$ for most of the calorimetry, but at coarser granularity in the end-caps and the forward region. These so-called *trigger towers* (TT) are formed by summing up the signals from up to 60 cells of the calorimeter, resulting in about 7200 analogue trigger towers (3584 for the electromagnetic calorimeter and the same amount for the hadronic calorimeter). Figure 3.4 shows the granularity of the calorimeters at trigger level. For technical reasons, it is coarser in the forward region, since the corresponding angle θ to the pseudorapidity η becomes very small for large values of η.

Due to attenuation from signal propagation within the cables, the signals are conditioned by the *Receivers Modules* (Rx), including a geometrical conversion of the signals from energy to transverse energy. The signals are digitised and calibrated by the PPr and distributed to the CP and JEP at their appropriate granularity (see sections 3.2.2, 3.2.3 and 3.2.4), where they are evaluated in parallel. The results from the CP and JEP are merged by the CMM and passed to the CTP. If the CTP emits a L1A, the RoI from CP and JEP are provided to Level-2 by the ROD modules, which in addition monitors all decision making and the condition of the system.
The whole system fills 14 9U[5] crates altogether. It is installed in the USA15 cavern, which is located right beside the detector and shielded by 2 m thick walls from the radiation of the

[5]9U - 1U is the standard unit in the VME specifications. 9U = 36.6 cm.

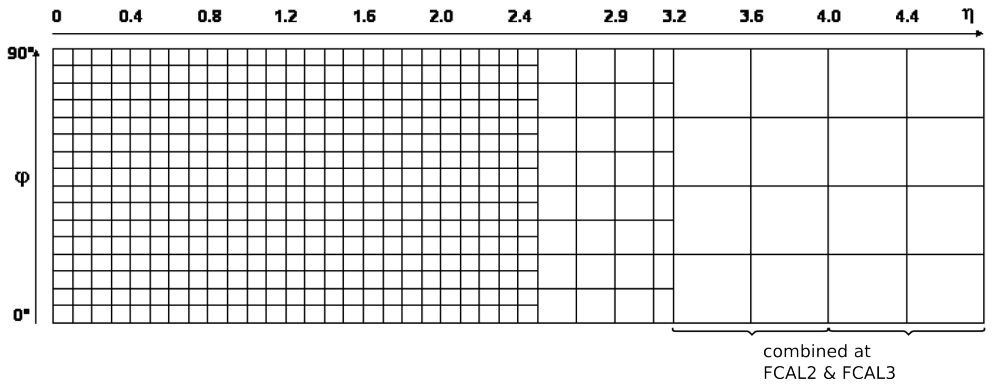


Figure 3.4: Trigger tower granularity of the electromagnetic calorimeter for $0 < \eta < 4.9$ and one quadrant in ϕ. The granularity for the hadronic calorimeter is slightly different in the forward region $3.2 < \eta < 4.9$.

proton-proton interactions, and thus is accessible also during detector operation.

The latency of the Level-1 Calorimeter Trigger amounts to $< 2.1\,\mu s$, which is well below the limit of $2.5\,\mu s$ given by the length of the pipeline memories of the detectors' side. Only a fraction of $< 1\,\mu s$ is consumed by the electronics, the main contingent is due to cable transmission delays and the delays from the receivers and the CTP.

3.2.1 The Analogue Signal Chain

The analogue signals of the 7200 projective trigger towers are summed on the detector and transmitted to L1Calo over 616 16-way twisted-pair cables[6]. The cable length varies between 30 m for the shortest LAr barrel cables and 70 m for the longest the TileCal cables, which corresponds to a transmission time of $142.8\,ns \hat{\approx} 6$ bunch crossings respectively $333.2\,ns \hat{\approx} 14$ bunch crossings assuming a propagation velocity of the signal of 4.76 ns/m. The resulting time variation of about $200\,ns \hat{\approx} 5$ bunch crossings needs to be corrected for on the PreProcessor side in order to identify a certain event with its corresponding bunch crossing.

The pulse shapes of the LAr-based detector elements and the shapes of the TileCal are very different as shown in the figures 3.5 and 3.6.

For the LAr, the pulse is shaped by bipolar shapers in order to minimise pile-up effects. It results in a charge balanced signal including a peak with a rise time of $\sim 50\,ns$ and a very characteristic undershoot of equal area with a length of another $\sim 350\,ns$. Hence the positive part of the pulse extends over 5 bunch crossings, which again has an important impact on the trigger architecture.

The TileCal signal is based on scintillation light that is detected and amplified by photo multiplier tubes, and thus much faster than the LAr signals. It has a FWHM[7] of typically 15 ns. In order to enable an equal processing of both LAr and TileCal signals, it is shaped to a unipolar pulse with a FWHM of about 50 ns similar to the LAr pulse shape as shown in figure 3.6. The shaping takes place on the detector right before the trigger towers are

[6]Twisted-pair cables consist of two twisted conductors with equal length. They are well suited to transmit differential signals since electromagnetic interference from external sources cancels out and crosstalk between neighbouring pairs is minimal.

[7]FWHM - full width at half maximum.

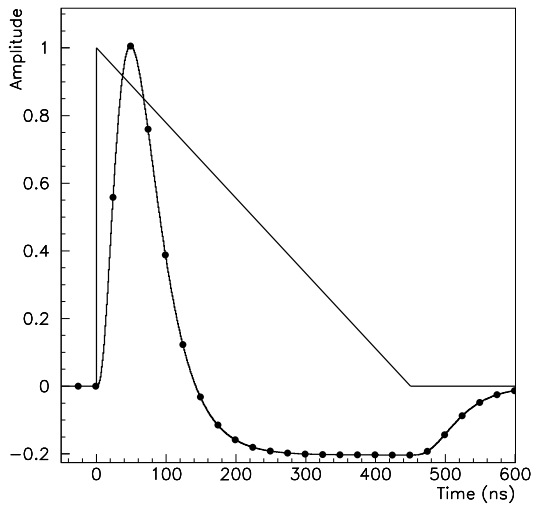


Figure 3.5: Ideal signal from the LAr calorimeter (straight line) and the corresponding pulse after shaping (line with dots; the dots indicate the sampling frequency of 40 MHz) [15].

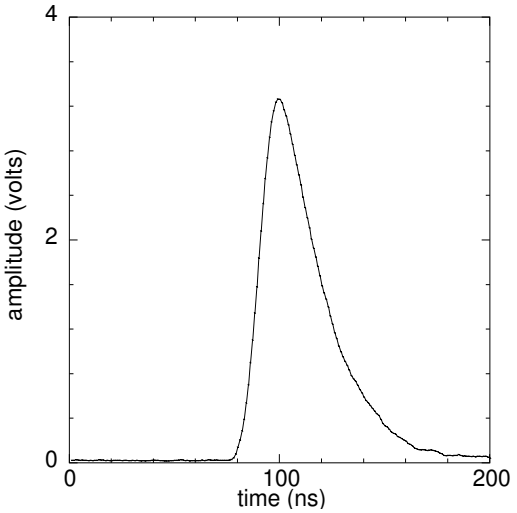


Figure 3.6: Signal from the tile calorimeter after shaping. The parameters were chosen such that it has a pulse shape similar to the LAr signal (figure on the left) [11].

composed from different readout cells.

All components of the signal chain have been chosen such that the crosstalk between neighbouring channels is below 0.5%. Hence a *standard pulse* as described above with a rise time of typically 50 ns and a peak voltage of maximal 2.5 V causes distortion on adjacent channels not above 12.5 mV. Therefore, the cables are also individually shielded in addition to their outer global shield.

Before finally reaching L1Calo, all trigger tower signals are passed through the Receiver Modules (Rx). They basically consist of linear variable-gain amplifiers controlled by DACs[8], which compensate for cable attenuation (up to 40% for the longest cables) and convert the hadronic trigger towers from energy E to E_{T}. The Rx provides monitoring for a small programmable selection of channels. Furthermore, the channels are remapped such that they comply to the architecture of the trigger. The Receiver Modules are located in USA15 and cover 8 crates: 6 for LAr and 2 for the Tile Calorimeter, each containing 16 receiver boards.

3.2.2 The PreProcessor System

The PreProcessor System performs several tasks in order to prepare the signals for the analysis in the subsequent modules, JEM and CP. Its tasks can be summarised as follows:

Converting and conditioning of the analogue signal. The incoming signals are transmitted differentially and have an amplitude of ±1.25 V. First, it is converted to a single-ended signal[9] with an amplitude of 2.5 V, including a calibration of the baseline using a programmable DAC (10-bit).

[8] DAC - digital-to-analogue converter.

[9] At single-ended signalling, one wire carries the signal while another represents the reference voltage, usually ground.

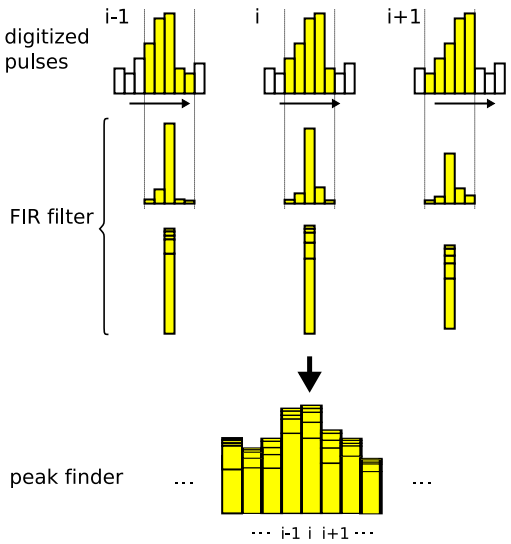


Figure 3.7: Illustration of the FIR filter process.

Digitisation and phase alignment. Each analogue signal is digitised by a 10-bit Flash ADC[10] at a sampling rate of 40 MHz. The clock of the FADC, thus the sampling phase, can be shifted by a programmable delay of 1 ns step size in order to sample the pulse at its maximum.

Timing and Bunch-Crossing Identification (BCID). One of the main tasks of the Pre-Processor is to associate the pulses with a certain bunch crossing. Since the signals arrive staggered at the trigger due to a varying time of flight of the particles from the interaction point to the detector and different lengths of the cables from the detector to the trigger electronics, they have to be aligned in time relatively to each other. Therefore, the output of the FADC is pipelined in a FIFO[11] buffer. As stated before, the delay from cables differs within 5 bunch crossings, so that the implemented FIFO with a depth of 16 bunch crossings can be considered as sufficient. The BCID logic evaluates the energy deposition E_{T} of the associated pulse. Since the pulse shapes from TileCal and the LAr detectors differ widely, exceed several bunch crossings and furthermore can also be saturated, a robust method for the energy estimation is required. Three methods are implemented:

- For non-saturated signals, a digital pipelined finite-impulse-response (FIR) filter is used. It makes use of the fact that the pulse shape of unsaturated pulses is independent of the amplitude, i.e. that the position of the peak is the same for all pulses. The method applies pre-defined coefficients to a set of five consecutive pulse samples to sharpen the pulse. Figure 3.7 illustrates the effect. Every 25 ns, the transverse energies of the five weighted samples are summed up to a 10-bit value, and the local maxima are subsequently associated with a certain bunch crossing.

[10] Flash ADC - Flash Analogue-to-Digital Converter (also FADC). It converts an analogue signal to discrete digital numbers by successively comparing the input voltage with the reference levels of a voltage ladder (an extensive voltage divider consisting of many resistors in series).

[11] FIFO - First In First Out.

This is the main method for pulses below the saturation limit of 256 GeV.

- Whenever trigger towers show saturated signals, all consecutive blocks of the Level-1 assume the energy to be at the maximum of their respective energy scale. Hence, the task on saturated signals is not to estimate the energy, but only the precise position in time when it occurred, which lies obviously somewhere within the samples that saturated. The BCID logic analyses the slope of the rising edge of the pulse based on two thresholds E_{low} and E_{high}. From the time interval between passing the two thresholds, the peaking time can be estimated well for energies above 200 GeV [9].
- The third method uses a threshold comparator to detect the rising edge of the pulse and adds a fixed, shaper-defined delay in order to estimate the peak time. The method is called external BCID and is introduced basically as cross-check for the other two methods.

Look-up-table (LUT). The 10-bit bit data is mapped to 8-bit values with a nominal energy of 1 GeV per count using a look-up-table, which can perform multiple tasks at the same time: E_{T} fine calibration (also the correction of non-linearities, if necessary) and pedestal subtraction in order to suppress noise.

Data transmission. The PPM provides two data streams to the subsequent modules, CP and JEP. Since the jet analysis algorithm uses a coarser granularity, a pre-summing is performed. Four trigger towers are summed up and transmitted as 0.2×0.2 elements in $\Delta\eta \times \Delta\phi$ to the Jet/Energy Processor. The data is transmitted using serial LVDS[12] links with a data rate of 400 MBit/s.

Monitoring. Apart from the real-time data path, the PPM provides monitoring tools in order to control the PPM with respect to trigger decisions, the electrical performance and the configuration of the PPM, and also to gain knowledge about the activity of the detector. Therefore, the PPM exhibits dedicated memories to record signal-rate histograms, and moreover the occurrences of energy deposition above a programmable threshold. The data collection at the PPM side has the big advantage that it is entirely free of trigger bias, i.e. no events have been discarded at this point. Therefore, it is the only tool that provides an in-situ monitoring of the whole calorimetry over time. This feature is called *Rate Metering and Histogramming* and is discussed in detail in chapter 4 as being the main topic of this thesis.

Implementation

The PreProcessor Module (PPM) is implemented as 9U printed circuit board[13] in a VME64xP crate environment. Every module processes 64 channels, 16 modules are grouped together in one crate (two crates have only 14 PPMs), and 8 crates are used in total. Each crate also contains a 6U VMEbus crate CPU module, which handles the communication for configuring and monitoring the modules, and a Timing Control Module (TCM) that provides the LHC 40 MHz clock and monitors voltages and temperatures of the modules via a CANbus (see section 3.2.2).

Figure 3.8 shows a photograph of a PPM. It consists of several submodules that are mounted

[12] LVDS - Low Voltage Differential Signalling.
[13] PCB - Printed Circuit Board.

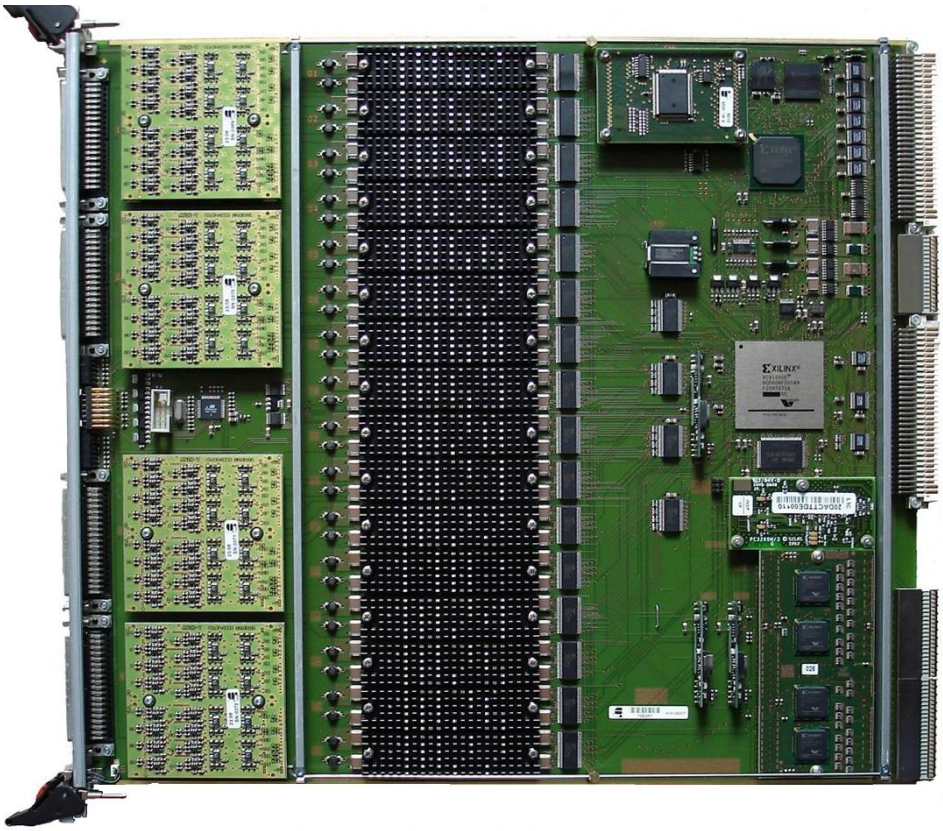


Figure 3.8: Photograph of the PreProcessor Module (PPM).

on a PCB, which basically performs the communication between submodules and their configuration, and also the communication to the VME bus. The modular approach allows for an easy service and replacement of defective hardware.

The signals are transmitted differentially in 16-way twisted-pair cables from the receiver modules and enter the PPM on four D-Sub 37c connectors on the front panel (left-hand side). From there, they are passed to the Analogue Input (AnIn) submodules, where they are converted to single-ended signals and conditioned for digitisation. The main signal processing takes place on the subsequent Multi-Chip Module (MCM): Digitisation, Timing, BCID and the LUT operations. Furthermore, the data are prepared for the transmission in the data streams to JEP and CP. Each MCM handles 4 channels at a time, thus 16 MCMs are mounted on each PPM. From there, the data is transmitted via LVDS Cable Drivers (LCD) to the VME backplane and subsequently via 4-pair cable assemblies of type AMP to JEM and CP. Figure 3.9 is a block diagram of the signal processing of one channel. The responsibility of the several submodules is indicated by the different colours.

Apart from this real-time data path, another data path for the trigger data acquisition (DAQ) is implemented. It is managed by the ReMFPGA (see 3.2.2). This chip is the master FPGA on the PPM and provides a VME interface for the configuration and readout of the submodules including monitoring. Furthermore, it communicates with the LHC TTC[14] respectively the TCM of the crate via the TTCdec submodule.

[14]TTC - Trigger and Timing Control system.

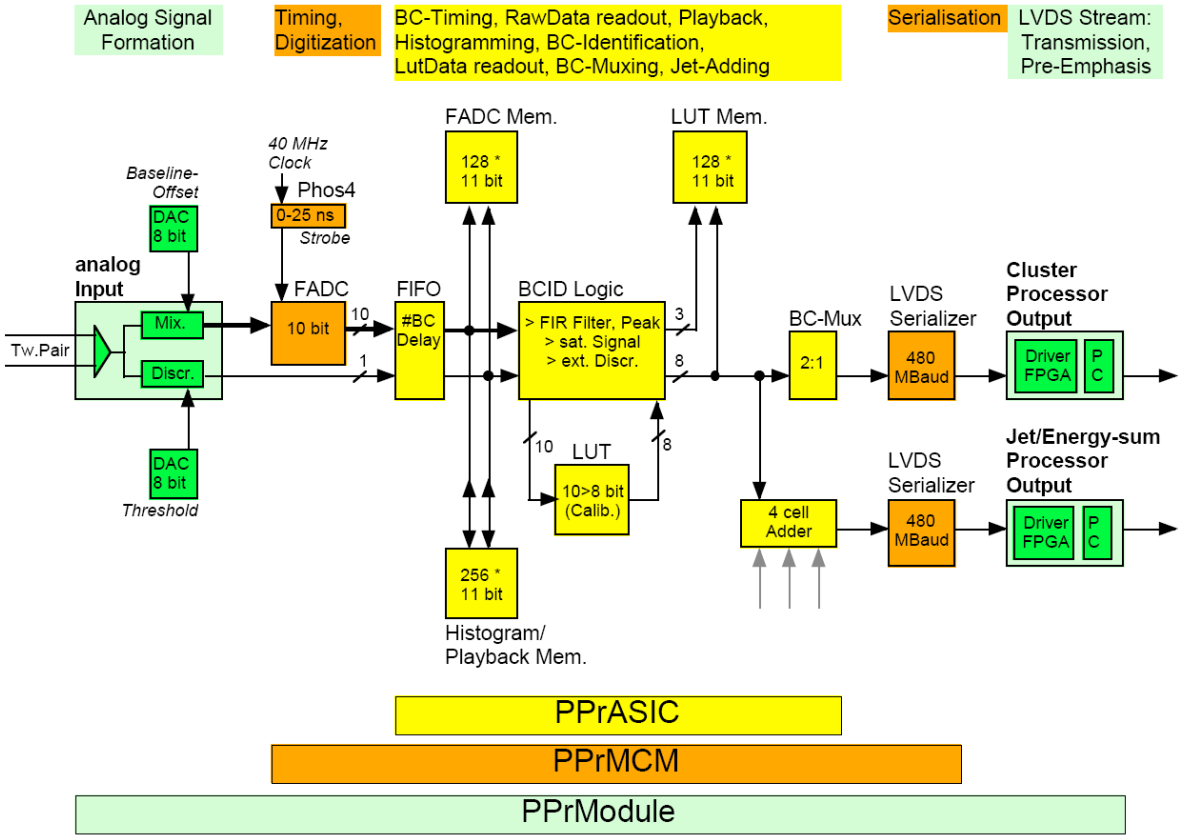


Figure 3.9: Block diagram of the signal processing of one channel on the PreProcessor Module [16].

Analogue Input Board (AnIn). 16 signals at a time are processed by one Analogue Input submodule (see figure 3.10), i.e. four AnIns are mounted on each PPM. The AnIn converts the signals from differential to single-ended, introducing an adjustable gain and a base line shift in order to suit the subsequent digitisation. It is chosen such that the digitisation FADC saturates for signals corresponding to 250 GeV, which is also the saturation energy of the trigger tower summation on the calorimeter. The input voltage range of the FADC is $U_{FADC} = [2.0, 3.0]$V, and since the amplitude of the incoming signal is $U_{max} = 2.5$ V, the gain was chosen as gain = 0.43 [17]. The value takes into account that the signal passes a low-pass filter before the digitisation which reduces the amplitude by about 20%. The base line shift is set by an 8-bit DAC with a 2.4 mV/step resolution and a range of $U_{offset} = [1.65, 2.26]$V. In addition, the AnIn evaluates the external BCID, i.e. the peaking time of the shaped calorimeter pulse in terms of bunch crossings. A comparator surveys the signal using a programmable threshold, which is set by an 8-bit DAC with a resolution of 10 mV, corresponding to ~ 1 GeV. Once the signal exceeds the threshold, a digital output signal of '1' is sent to the MCM, and '0' otherwise. The bunch crossing identification is then performed by the PPrASIC, as described in a later stage of this section.

The Multi-Chip Module (MCM). The MCM is the main functional block of the PPr. Its major task is to process four single-ended signals each from the AnIn, and to deliver

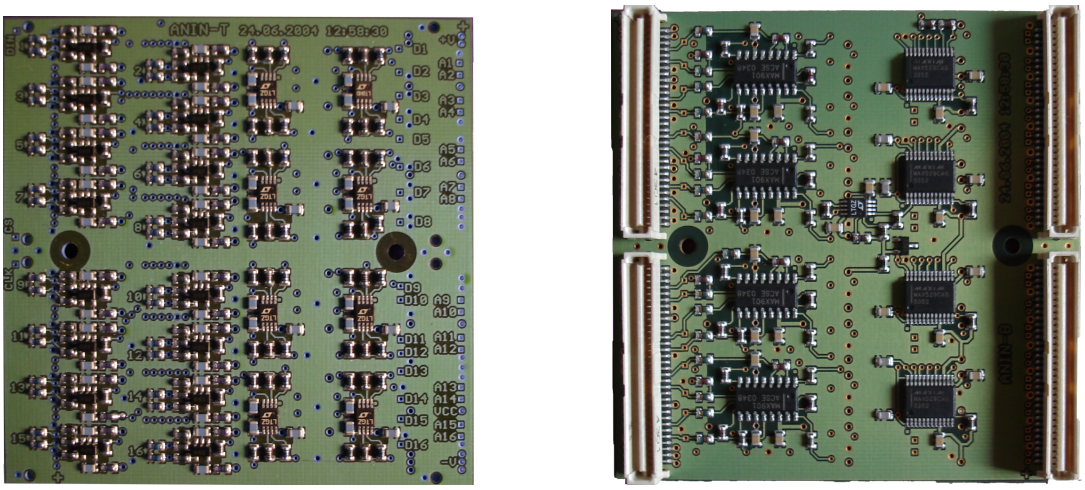


Figure 3.10: Top (left) and bottom view (right) of the AnIn Board.

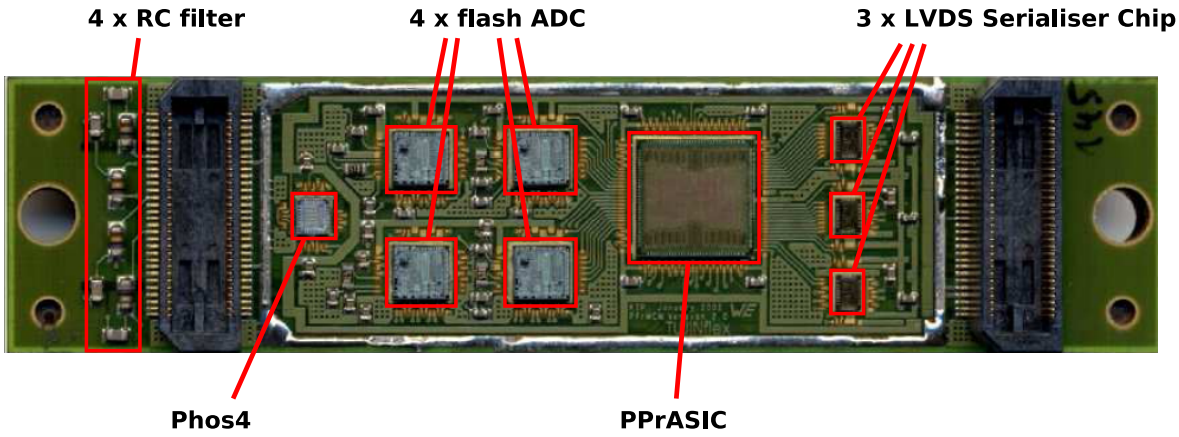


Figure 3.11: Photograph of the PreProcessor Multi-Chip Module without its cover.

digitised data containing the calibrated transverse energy to both, JEP and CP in a serial data stream. Figure 3.11 is a photograph of a MCM where the covering brass-lid and the *glob-top*[15] are removed. It is a compact electronic module consisting of a substrate on which nine dies[16] are assembled: four FADCs to digitise the signals, the Phos4 chip for a phase adjustment of the FADC sampling, the PPrASIC as the major logic block, and three LVDS Serialiser Chips.

The signal path is from left to right, starting with a low-pass filter for four channels in parallel to reduce high frequency noise before the digitisation, which leads to a decrease of amplitude by about 20%. This is taken into account by the AnIn board. Four FADCs digitise the signals with a 10-bit resolution at an input voltage range of $U_{FADC} = [2.0, 3.0]V$, hence with a step size of about 1mV. The sampling rate of the signal is the bunch crossing frequency

[15]Glob-top is a type of protection from environmental, mechanical and electrical damage used in chip-on-board assembly. It consists of a small portion of specially formulated resin that covers the die and the bond wires.

[16]die - chip without packaging.

of 40 MHz $\leftrightarrow$ 25 ns, but the phase can be shifted by a programmable delay of 1 ns step size in order to sample the pulse at its maximum. The Phos4 chip, developed by the CERN Microelectronics Group, performs this task. The digitised signal enters the PPrASIC, which performs the major logic operations: real-time BCID, channel synchronisation with a FIFO to pipeline the signal for an adjustable time interval, final transverse energy calibration and pedestal subtraction using a LUT, the pre-summing of the jet elements to a coarser granularity of 2×2 trigger towers as needed by the JEP, and serial data transmission. Moreover, it performs monitoring tasks. The PPrASIC is described in detail in the next paragraph.
From there, the data is transmitted via a 10-bit data bus to three LVDS Serialiser Chips: one provides pre-summed trigger towers to the Jet-Energy Processor (it processes data at a coarser granularity of 2×2 trigger towers), while the other two supply the Cluster Processor. Since four trigger towers have to be transmitted to the CP in parallel, a 2:1 multiplexing scheme was implemented in the PPrASIC. The serialisers achieve a data rate of 400 Mbit/s.

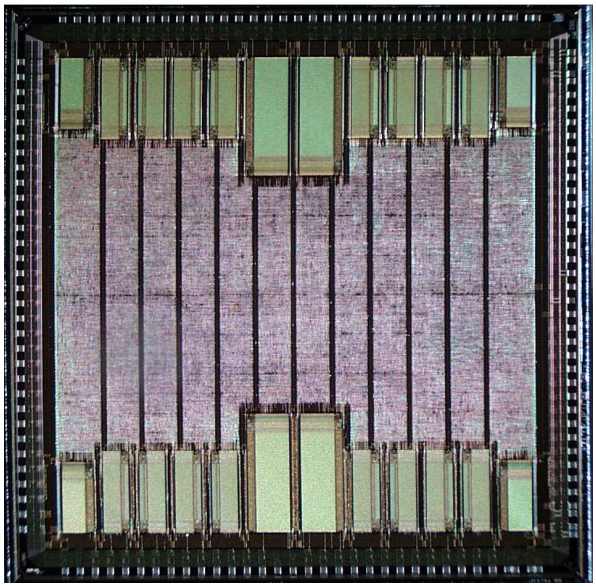


Figure 3.12: Photograph of the PPrASIC.

PPrASIC. The PPrASIC is the key component of the Level-1 PreProcessor system. *ASIC* stands for *application-specific integrated circuit* and is a customised integrated circuit that is built for a particular use - the data processing of the incoming digitised trigger tower signals. The development of such a customised chip was mandatory in the case of the PreProcessor System in order to be able to perform the required tasks in a reasonable time.
The chip was designed in the ASIC laboratory of the Kirchhoff-Institute for Physics in Heidelberg and submitted for production in 2002. 3130 MCMs have been produced to cover the required 1984 modules in total on all 124 PPMs.
The chip was implemented with 0.6 µm CMOS[17] technology on a die with a size of 68.89 mm^2, consisting of 990 000 transistors and 8.125 kByte RAM[18]. Figure 3.12 is a photograph of the die. The symmetry is such that each quadrant is dedicated to one of the four channels that

[17] CMOS - Complementary MetalOxideSemiconductor.
[18] RAM - Random Access Memory.

are processed on the MCM. The green blocks are the memory blocks, the purple area contains the logic.
Referring to the block diagram in figure 3.9, the central tasks are timing (FIFO, BCID logic) and energy calibration (LUT). As stated in section 3.2.1, the transmission time differs through variable cable length and time of flight. The PPrASIC performs the time alignment of the signals relatively to each other. It should be mentioned that the timing of the entire Level-1 Calorimeter Trigger system is based on the fact that both transmission times from the detector to the Level-1 and between the subsystems are constant, since it is a pipelined system based on the LHC bunch crossing frequency of 40 MHz with fixed delays for each system in terms of clock ticks. Once the delays are known, they can be compensated by introducing the corresponding number of clock ticks to the FIFO that is implemented on the PPrASIC.
The other task on the timing issue is the determination of the bunch crossing in which the calorimeter signal reaches its maximum amplitude. Two algorithms of that so-called bunch crossing identification are implemented on the PPrASIC and work in parallel: the one for non-saturated pulses, which are evaluated by applying a FIR filter and a consecutive peak finding, and one for saturated pulses as described in section 3.2.2. In addition, the external BCID being the third algorithm and performed mainly by the AnIn is taken into account. Which method is used is decided by a LUT that contains programmable energy intervals for each method.
The digital signal enters the PPrASIC with a resolution of 10-bit and is mapped to the final 8-bit trigger tower resolution using another LUT. It consists of a 1024×8 bit memory and allows for a flexible calibration of the transverse energy including a pedestal[19] subtraction to suppress noise.

Readout Merger FPGA (ReMFPGA). The Readout Merger FPGA manages the data transmission on the PreProcessor Module, i.e. the complete read/write access of all configurable settings by the crate CPU module via the VMEbus on the one hand and the onboard communication with the submodules of the PPM on the other. The latter consists of the configuration of registers, the readout of registers in order to verify the settings, and the monitoring stream for both event-related results, which are provided to the ATLAS Data Acquisition (DAQ), and general monitoring functionalities of the PPM (see chapter 4). When necessary, the data is formatted by the so-called Readout Merger (ReM) sub-block. A detailed description of the ReMFPGA can be found in [16].

Controller Area Network (CAN). The CAN surveys the board conditions like temperature, supply voltages, currents etc. in order to guarantee a reliable system operation and to report emerging failures. The obtained information is provided to the Detector Control System (DCS) via the CANbus [18].

3.2.3 The Cluster Processor

The cluster processor performs a search for isolated electrons and photons as well as hadronic τ decays using a *sliding window* algorithm. It is based on the evaluation of the energy depositions in a predefined, relatively small area. The result is associated to the center coordinate of that window, and by sliding the window over the entire η/ϕ range in every available position,

[19] A pedestal means a constant value respective base line.

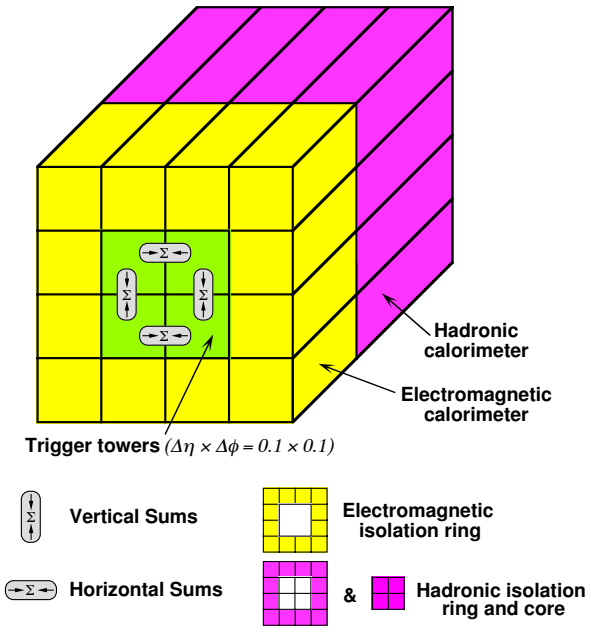


Figure 3.13: Illustration of the CP sliding window.

the whole detector is covered. The window consists of 16 adjacent trigger towers as shown in figure 3.13, with a size of 4×4 TTs in $\eta \times \phi$ for both electromagnetic and hadronic calorimeter independently.
The identification of e/γ and hadronic decaying τ is similar, but not identical: electrons and photons initiate compact electromagnetic showers which penetrate only into the electromagnetic calorimeter, whereas the hadronic τ decay products also deposit energy in the hadronic layer. However, both algorithms search for relatively narrow showers in the EM calorimeter that do not exceed more than two neighbouring trigger towers. Therefore, the combinations of two adjacent trigger towers in the center of the sliding window 1×2 and 2×1 are considered. The e/γ algorithm requests that the sum of E_{T} of any of the combinations passes a threshold $E_{\mathrm{T}}^{\mathrm{Cluster}}$, while the energy sum of the 2×2 core region of the hadronic calorimeter must remain below a threshold $E_{\mathrm{T}}^{\mathrm{hadronic\ veto}}$. The τ-algorithm in contrast requires that the sum of both, the sum of the transverse energy of two adjacent trigger towers of the EM layer and the sum of the projective 2×2 hadronic core region of the hadronic layer, exceed the threshold $E_{\mathrm{T}}^{\mathrm{tau}}$. Furthermore, an isolation criterion is estimated by evaluating the sum of the 12 surrounding trigger towers of the 2×2 core region in either the EM and the hadronic layer with the respective thresholds $E_{\mathrm{T}}^{\mathrm{EM\ isolation}}$ and $E_{\mathrm{T}}^{\mathrm{had\ isolation}}$. All thresholds are programmable and can be deactivated, too. 16 sets of cluster thresholds and isolation conditions are available and evaluated in parallel in the CP, including a combination to identify saturated channels.

Since the sliding windows overlap, trigger towers with high energies and especially saturated channels fulfil the algorithms' requirements in more than one window. In order to avoid multiple counting, the sum of the 2×2 core region of every sliding window is compared with the neighbouring windows and evaluated in terms of a local maximum as illustrated in figure 3.14. Although the e/γ algorithm would in principle only require the evaluation of the EM layer of the core region, the detection of local maxima is done identically for both e/γ and τ-algorithm by building the projective trigger of the EM *and* the hadronic calorimeter as it is not significantly decreasing the performance.

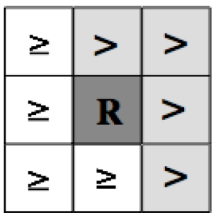


Figure 3.14: Local maximum test.

The Cluster Processor is implemented on the Cluster Processor Modules (CPMs), whose architecture is based on massive FPGA use. Every module processes 64 channels, and 56 modules are necessary in total. They are grouped in 4 crates, each covering one quadrant of the calorimeter. The results of the CPMs are collected and merged by two CMMs each crate, which provide the RoIs to the CTP and in addition single out ambiguities of trigger candidates that are detected on adjacent TTs of two CPMs. This is necessary since every CPM only covers 90° in ϕ and a relatively narrow slice in η, and no direct communication between CPMs is implemented.

3.2.4 The Jet/Energy-Sum Processor

The Jet/Energy-Sum Processor (JEP) performs jet finding and calculates the missing-E_{T} and total-E_{T}. Since jets cover a larger area than isolated particles and also penetrate the whole depth of the calorimeter, the JEP combines the electromagnetic and the hadronic layers and furthermore processes the data at a reduced granularity of mostly 0.2×0.2 in $\Delta\eta \times \Delta\phi$, the so-called *jet elements*. In order to be able to estimate $\sum E_{\mathrm{T}}^{\mathrm{miss}}$ and $\sum E_{\mathrm{T}}$, the JEP covers the entire range of $-4.9 < \eta < 4.9$ for the energy sum calculation, but $-3.2 < \eta < 3.2$ for the jet finding algorithms.

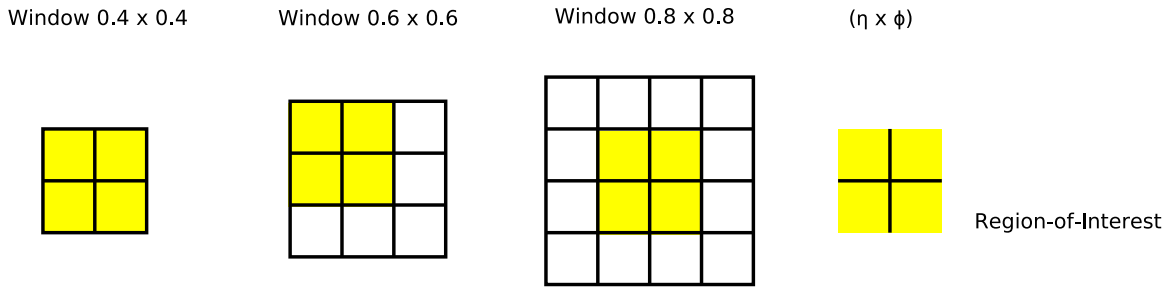


Figure 3.15: The sliding window of the jet finding algorithm.

Jet Finding Algorithm. The jet algorithm uses a technique similar to the CP sliding window, but with various window sizes of 2×2, 3×3 and 4×4 jet elements as shown in figure 3.15 and individual thresholds for the energy sum. The size is related to the desired multiplicity of jets. While in a larger window, the efficiency of finding jets is higher since

the window contains more energy depositions and therefore covers a greater amount of the jet, a smaller window size is preferred for resolving multiple jets. In order to avoid multiple counting of the same jet, a local maximum in the sum of E_{T} of a 2×2 subset of jet elements is required. In fact, the search for that local maximum is done even before the estimation of the energy sum of the larger 3×3 and 4×4 windows since it simplifies the implementation without affecting the efficiency. As ambiguities occur applying the 3×3 in one of the 4 possible positions around the 2×2 core region, the combination with the highest sum of E_{T} is chosen. Furthermore, the center of the core region indicates the RoI and is passed to the Level-2 trigger in case of a positive trigger decision. The sums of E_{T} are compared with a 10-bit threshold with a nominal resolution of one count per GeV. Eight independent sets of threshold/window size combination are available.

The JEP system consists of 32 *Jet Energy Modules* (JEMs), housed in two crates. Every crate also comprises two CMMs to merge the results from 16 JEMs. This includes sorting of ambiguities, providing the RoI to the Level-2, energy sum calculation (see next paragraph) and monitoring of the decision making and system operation.

Energy Sum and Missing Energy. The calculation of the energy sums $E_{\mathrm{T}}^{\mathrm{miss}}$ and E_{T} is done partially on the JEM and on the CMM. The JEM provides the sum of E_{T} as a 12-bit value (4095 GeV) to the CMM, and also the vectorial components E_x and E_y depending on the position of the trigger tower for the calculation of the missing energy. The CMM combines the output of the JEM, performs threshold comparison and passes the results to the CTP.

Chapter 4

Rate Metering and Histogramming

4.1 Introduction and Motivation

The Rate Metering and Histogramming feature of the PPrASIC provides an essential monitoring of the activity of the electromagnetic and hadronic calorimeter of the ATLAS detector at trigger level. It is based on the evaluation of the transverse energy for every trigger tower independently, i.e. for all 7 200 channels.

The idea of Rate Metering is to evaluate the energy depositions in the calorimeter over a given time interval with respect to a programmable threshold. Whenever a signal exceeds $E_{\mathrm{T,\ thresh}}$, a signal counter is incremented as illustrated in figure 4.1.
Similarly, the Histogramming feature monitors the transverse energy spectrum in every trigger tower. It maps the digitised transverse energies to a histogram such that every bin of the histogram corresponds to an energy value, as shown in figure 4.2.

Since both Rate Metering and Histogramming are obtained at a point of the signal processing chain where no events are discarded by the trigger decision, the rates are entirely free of trigger bias and provide valuable information about the performance of the calorimetry with high statistics[1]:

Diagnostic purposes. Displaying the rates e.g. as a 2-dimensional colour map, which can be used to identify faulty channels from dead or hot calorimeter cells. Additionally, the Histogramming feature provides the averaged energy spectra and allows for the analysis of systematically odd behaving channels.

Calibration. The energy distribution in the detector is uniform in ϕ, supposing a perfect detector and beam alignment, of course. Moreover, the energy distribution in η and ϕ can be predicted from simulations. Taking this into account, an in-situ calibration of the trigger tower energies can be achieved using the high statistics from the unbiased rates of the Rate Metering and Histogramming [17].

Beam quality. Since the Rate Metering shows the overall distribution of energy depositions in the detector, it should be possible to draw conclusions on the beam quality like beam shift or beam halo[2] from e.g. an asymmetric distribution.

[1] In principle, this could also be achieved with *random triggers*, but since the rates are rather low (see 4.4), it would only obtain poor statistics.

[2] Beam halo denotes parasitic particles that surround the beam core region.

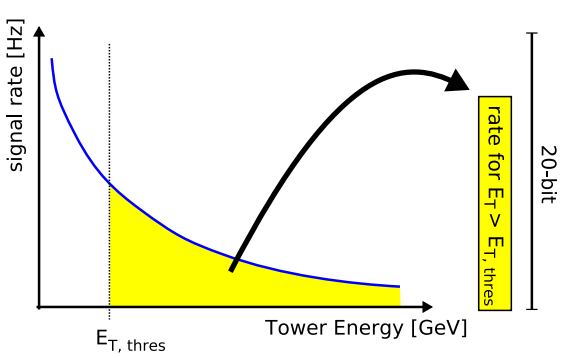


Figure 4.1: Illustration of the Rate Metering functionality of the PreProcessor. A 20-bit register holds the rate count.

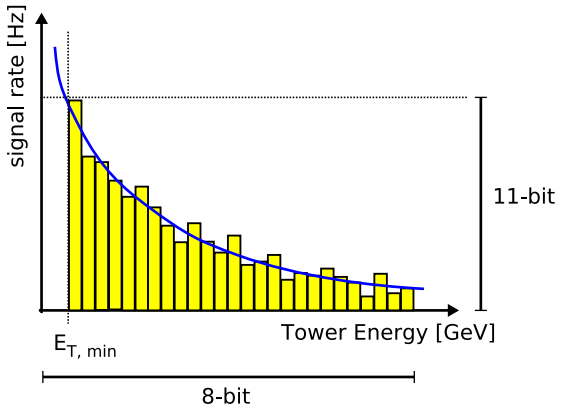


Figure 4.2: Illustration of the Histogramming functionality of the PreProcessor. The energy rate is stored in 11-bit words in an 8-bit address range.

In principle, the rates of the Rate Metering could be obtained from the histograms, but since the Histrogramming feature is very memory consuming in contrast to the Rate Metering and the readout bandwidth is limited, a frequent readout of the energy spectra is not possible. Therefore, the histograms are read out only occasionally, whereas the Rate Metering functionality is used for a continuous monitoring and e.g. a visual representation as a 2-dimensional histogram of the η-ϕ plane containing the rates (signal counts/time). Depending on the threshold respective the instantaneous luminosity, this map can be updated with moderate frequencies in order to obtain a quasi-instantaneous monitor of the calorimeter activity.

The following chapters focus on the analysis of the signal rates for the Rate Metering and Histogramming. The estimation of the signal rates as expected in the experiment is mandatory for a reasonable energy thresholds and readout frequency configuration.

4.2 Implementation

The Rate Metering and Histogramming feature was proposed in 1999 and implemented in the PPrASIC logic. For the Rate Metering, a 20-bit signal counter holds the number of energy deposits above the adjustable threshold. The input can be either the raw digitised FADC value (10-bit) or the BCID calibrated energy (8-bit). In order to cover the entire dynamic range of the FADC, the threshold is a 10-bit register[3].

The time interval is estimated in terms of LHC bunch crossings, but with a reduced resolution of 25 µs[4] since this is considered as sufficient and reduces significantly the width of the time register. Therefore, the time counter is twofold: a 10-bit counter (scaler) that is incremented with the LHC bunch crossing frequency, and a 16-bit counter that is incremented by the scaler overflow. Hence, the 16-bit counter contains the time value in units of 25 µs. Another 16-bit counter holds a programmable time interval to trigger the stop of the counting.

[3]In case that the BCID calibrated energies are used as input, the BCID value is extended to a 10-bit word by adding two bits as LSBs set to zero.

[4]The exact value is 25.575 µs.

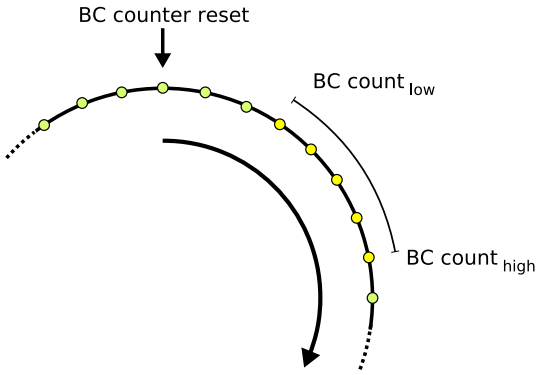


Figure 4.3: Illustration of the Histogramming measuring window.

The time counter limits the maximum time span between consecutive readouts, which is $2^{10} \cdot 2^{16} \cdot 25\,\text{ns} = 1.68\,\text{s}$. Besides, the counting also stops when the signal counter experiences an overflow.

The Histogramming memory has an 8-bit address range with 11-bit words, i.e. 256 energy bins are available with a maximum count of 2 047 each. Figure 4.2 illustrates a typical energy spectrum. The bin width and the energy range of the histogram are adjustable from 250 MeV/bin to 1 GeV/bin, including a programmable minimum energy threshold (10-bit) to suppress contribution from noise at low energies in order to prevent a fast overflow in that range. The Histogramming feature can be applied to a certain number of bunch crossings exclusively. Two 12-bit registers define the lower and upper boundary of a measuring window in terms of bunch crossings. Figure 4.3 illustrates the measuring window.

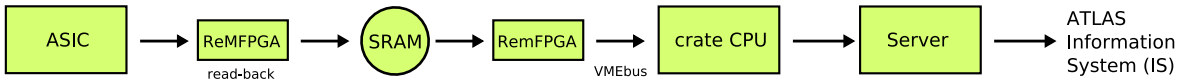


Figure 4.4: Scheme of a possible Rate Metering and Histogramming readout concept.

The readout of the Rate Metering and Histrogramming data is a multi-stage process. Figure 4.4 shows a possible concept for the realisation. It starts on the PPrASIC with the *read-back* of the register and memory blocks that contain the actual data to the SRAM memory on the PPM. Details of the read-back can be found in [19]. The data is stored in the SRAM until a request from the crate CPU initiates the further readout via the VMEbus. There, the rates and histograms of a crate are gathered and provided to a central server, which holds the data of the whole PPr System and makes it available to the *ATLAS Information System* (IS).

4.3 Simulation of Expected Rates

Physics Simulation

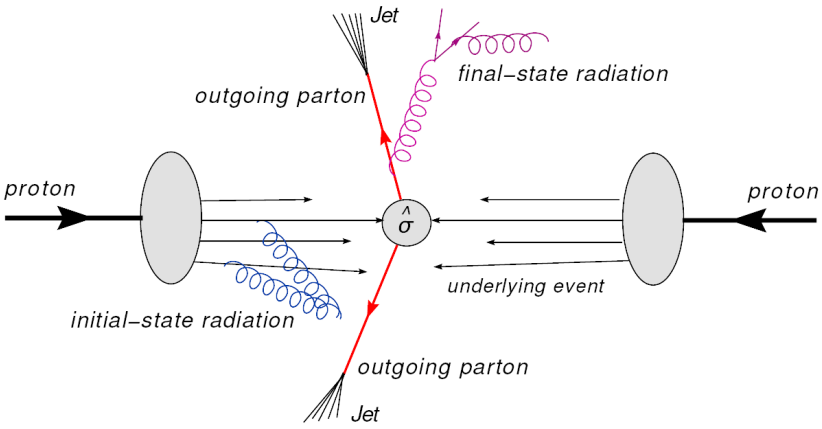


Figure 4.5: Inclusive jet production. Two jets emerge from the hard scattering of the primary particles. In addition, underlying events and initial- and final-state radiation occur (from [17]).

The study is based on the analysis of Monte-Carlo generated dijet events, which are the predominant processes in proton-proton scattering at the LHC. Figure 4.5 illustrates the process: two partons of the colliding proton bunches interact in a hard scattering with high transverse momentum p_{T} of the outgoing partons. Both partons hadronise quasi-instantaneously and form two jets in a back-to-back configuration in the azimuthal angle ϕ. In addition to the hard scattering process, initial and final state radiation as well as the soft underlying events, multiple interactions and minimum bias events are accounted for in the simulation.

Data Source

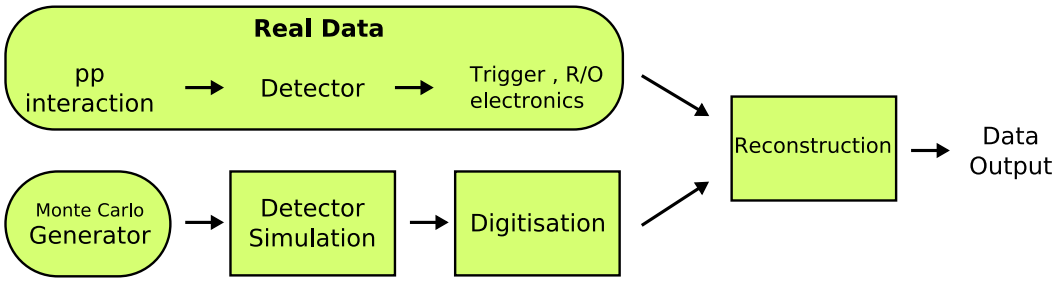


Figure 4.6: Simplified scheme of the processing chain.

The production of event data comprises several procedures. The first is the simulation of the dijet process with Monte-Carlo (MC) generators. Pythia [20] was used to simulate both the hard scattering process with the emerging jets and the soft scattering processes. The detector simulation is performed using the GEANT4 package [21], which is the toolkit for simulating the detector effects, i.e. the passage of particles through the detector medium,

but also to simulate the digitisation of the signals in the readout electronics. The resulting data has the same qualities like real data as expected from the running experiment.

The data is processed by the reconstruction stage, which consists of several procedures to extract physics objects like isolated particles, jets or $E_{\mathrm{T}}^{\mathrm{miss}}$ with their respective kinematic parameters ($E, \vec{p}$, etc.) from the data as received from the detector. Since the data also contains all detector effects, the reconstruction must take into account absorption processes by passive material, the detector misalignment and instrumental effects like electronic noise. Figure 4.6 is a simplified scheme of the processing chain.

The operations are embedded in the *Athena* software framework [22]. The output is available in several formats, of which ESD and AOD are the most common. ESDs (Event Summary Data) contain the detailed output of the reconstruction, i.e. information at cell level, tracking information, jet constituents and trigger data along with the MC truth information[5] in case of simulated events. AODs (Analysis Object Data) on the other hand include the refined reconstruction information in terms of identified particles and e.g. reconstructed jets. From either ESDs or AODs, a set of the relevant variables is extracted and written in so-called *ntuples*, which are the basis for the further analysis.

The production cross section of jets varies within several orders of magnitude since $\frac{d\sigma}{dp_{\mathrm{T}}} \sim E^{-5}$ [23]. In order to achieve sufficient statistics also in the high p_{T} region, the generation of simulated events is divided into different energy ranges. These subranges are defined by cuts on the transverse momentum on the hard scattering process, i.e.

$$p_{\mathrm{T,\,low}} < p_{\mathrm{T}} < p_{\mathrm{T,\,high}}.$$

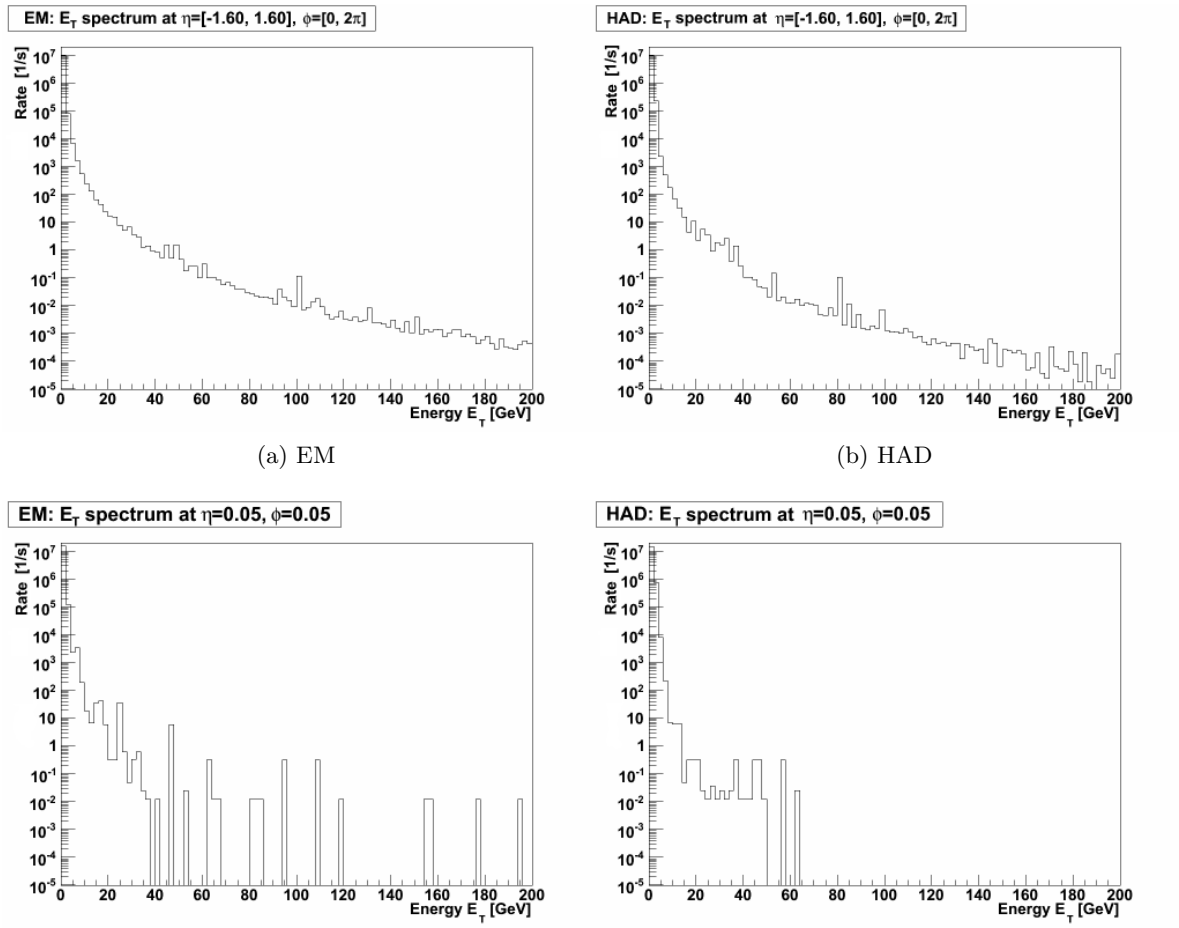
However, the energy spectrum of the reconstructed jets is not restricted on the defined p_{T}-region, since the soft scattering processes *initial state radiation* (ISR) and *finite state radiation* (FSR) smear the p_{T}-boundaries of the produced jets. Moreover, ISR, FSR, underlying and minimum bias events cause additional entries particularly at the low region of the p_{T} spectrum since additional particles with low energies are created.

In addition to the effects at generator level, the detector simulation and digitisation stages induce further modification of the spectrum, primarily due to the calorimeter resolution with a factor of $\Delta E/E \propto 1/\sqrt{E}$ and electronic noise. Of course, this affects particularly the low energy region samples.

data set	p_{T}-range [GeV]	cross section σ [pb]	#events	weights
J0	8-17	$1.76 \cdot 10^{10}$	78 938	2230
J1	17-35	$1.376 \cdot 10^{9}$	66 000	208.5
J2	35-70	$9.327 \cdot 10^{7}$	26 000	35.87
J3	70-140	$5.884 \cdot 10^{6}$	10 000	5.884
J4	140-280	$3.084 \cdot 10^{5}$	10 000	0.3084
J5	280-560	$1.247 \cdot 10^{4}$	10 000	0.01247
J6	560-1120	$3.44 \cdot 10^{3}$	-	-

Table 4.1: QCD dijet samples with their cross section and the corresponding weights.

[5] *Truth information* denotes the original kinematic parameters of the simulated particles at generator level unbiased from further interaction and detector effects.



(a) EM (b) HAD

(c) EM (d) HAD

Figure 4.7: Energy spectra of E_{T} for the central region $\eta = [-1.6, 1.6]$, $\phi = [0, 2\pi]$ (a), (b) and for a single bin with $\eta = 0.05$, $\phi = 0.05$ (c), (d) for a luminosity of $\mathcal{L}_{\mathrm{inst}} = 10^{34} \frac{1}{\mathrm{cm}^2\mathrm{s}}$.

To each sample a weight is assigned according to the respective cross section of the energy range and the number of events. Table 4.1 shows the borders on the used p_{T}-regions and the corresponding cross section, the number of used events for this study and the respective weight.

Since the threshold energy for the Rate Metering is expected to be below 50 GeV, 10 000 events are considered to be sufficient for J3, J4, and J5. Higher energy regions are ignored as the cross sections is several orders of magnitudes smaller and do not contribute to the rates significantly.

The ntuples were produced with Athena version 13.1.0, since it includes the trigger simulation. The relevant variables are the digitised and calibrated transverse energy E_{T} on trigger level for both the electromagnetic and the hadronic calorimeters as well as their coordinates in η and ϕ respective the channels on hardware level as received by the PreProcessor hardware.

Energy spectra

The resulting energy spectrum for the electromagnetic and the hadronic calorimeter is shown in figure 4.7 (a), (b) as the average spectrum in the region of $-1.6 < \eta < 1.6$ for the design luminosity of $\mathcal{L}_{\text{inst}} = 10^{34} \frac{1}{\text{cm}^2\text{s}}$. The energy spectrum shows the typical $\sim E^{-5}$ behaviour.

Figures 4.7 (c), (d) are the energy spectra for a single bin. The distribution shows large fluctuations and only very few entries for high energies. The latter is due to the low cross section in the high p_{T} region as mentioned above, whereas the statistical fluctuation might be caused by few events with large contribution from soft underlying events.

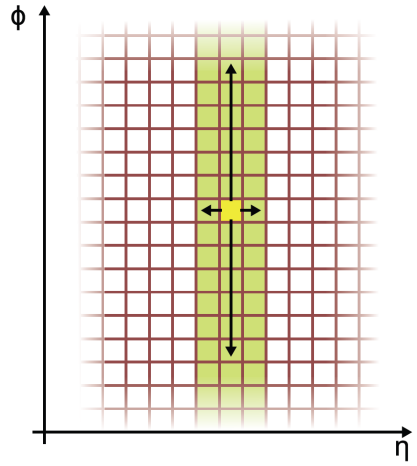


Figure 4.8: Illustration of the randomising process. In order to smooth the distribution, energy depositions are filled n-times redistributed over $0 < \phi < 2\pi$ and $|\Delta\eta| \leq 1$.

This effect is antagonised by smoothing the energy distribution in a two-part process as illustrated in figure 4.8:

1. No effects in the current simulation suggest an asymmetry in ϕ, and since the physics processes are expected to be ϕ-symmetric, every event is redistributed over the ϕ-range $[0, 2\pi]$ n_i-times. n_i is chosen individually for each sample J_i such that the weights of the samples become approximately equal. But since the cross section varies over several orders of magnitude, this could only be achieved for the low energy samples.

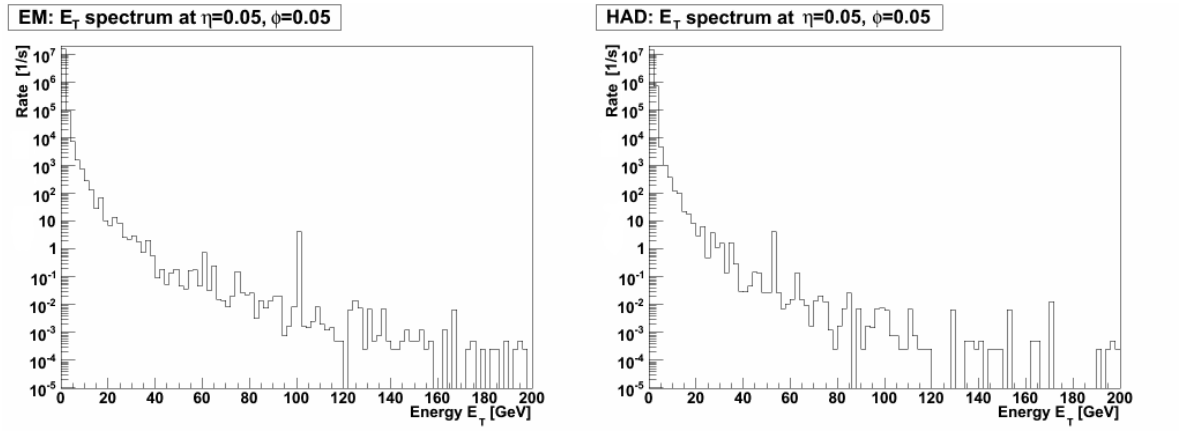
2. For the high granularity of the detector, variations of the energy distribution in η can be considered small. Therefore, every event is additionally redistributed in η to the adjacent bins ($|\Delta\eta| \leq 1$).

Thus the energy spectrum of a single bin is filled with entries from a surrounding area of up to $64 \cdot 3 - 1$ bins, so that single outliers are not significant any more. Although the energy distribution in a single bin is smoothed, it should be noted that the overall energy spectrum is conserved, since no new events are created. The number of events after the redistribution is shown in table 4.2.

Figure 4.9 shows the energy spectrum of the same bin as before, but with the redistribution method. The spectrum is smoother, and the outstanding bins are now embedded in a rather continuous distribution.
The method is not applied on FCAL2 and FCAL3, since they obtain satisfying statistics anyway due to their coarser granularity.

data set	cross section σ [pb]	#events MC	weight	#events redistributed	weight
J0	$1.76 \cdot 10^{10}$	78 938	2230	$3.95 \cdot 10^{7}$	4.46
J1	$1.376 \cdot 10^{9}$	66 000	208.5	$3.30 \cdot 10^{6}$	4.17
J2	$9.327 \cdot 10^{7}$	26 000	35.87	$1.30 \cdot 10^{6}$	$7.18 \cdot 10^{-1}$
J3	$5.884 \cdot 10^{6}$	10 000	5.884	500 000	$1.18 \cdot 10^{-2}$
J4	$3.084 \cdot 10^{5}$	10 000	0.3084	500 000	$6.17 \cdot 10^{-3}$
J5	$1.247 \cdot 10^{4}$	10 000	0.01247	500 000	$2.49 \cdot 10^{-4}$

Table 4.2: Redistribution of Monte-Carlo generated events to smooth the energy distribution. By multiple filling of events, the weights are reduced.



(a) EM (b) HAD

Figure 4.9: Energy spectrum for $\eta = 0.05$, $\phi = 0.05$ after *re-randomisation* (see text).

4.4 Expected Rates

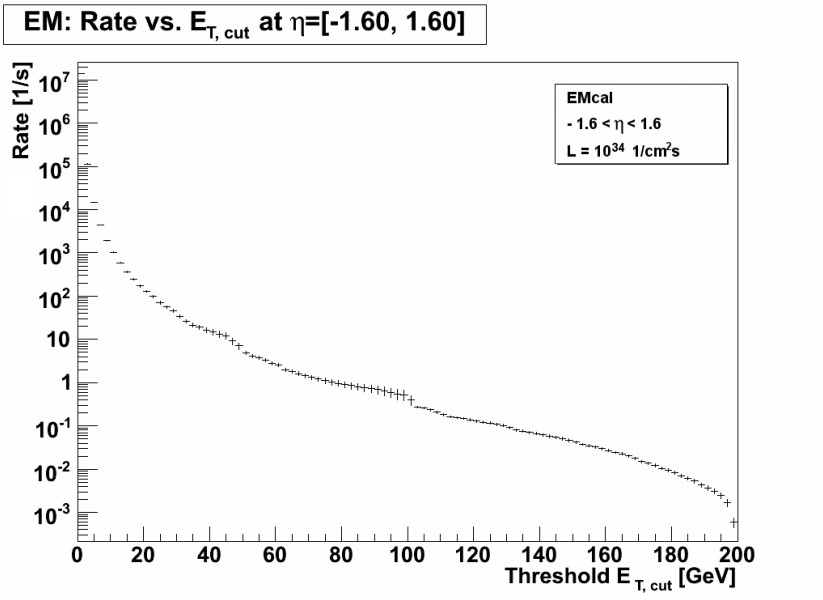
The rates for the Rate Metering are obtained from the energy spectra by summing the events that exceed the given threshold energy $E_{\mathrm{T,\ thresh}}$:

$$\text{rate} = \int_{E_{\mathrm{T,\ thresh}}}^{\infty} \frac{dN(E_{\mathrm{T}})}{dt} dE_{\mathrm{T}} \tag{4.1}$$

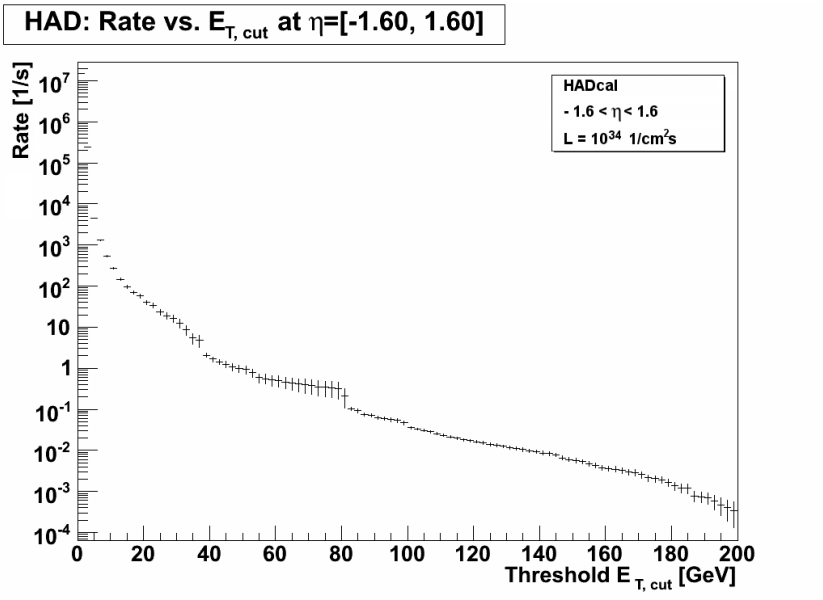
Figure 4.10 shows the dependency of the rate as a function of the energy threshold $E_{\mathrm{T,\ thresh}}$ in the central region for a luminosity of $\mathcal{L}_{\mathrm{inst}} = 10^{34} \frac{1}{\mathrm{cm}^2 s}$. As expected from $\frac{d\sigma}{dp_{\mathrm{T}}} \sim E^{-5}$ and (4.1), the rates drop down with increasing energies proportional to E^{-4}.

The result is authoritative for the adequate choice of the energy threshold with respect to the given purpose. Additionally, the following factors have to be taken into account:

1. The LHC will start its operation with a luminosity of $\mathcal{L}_{\mathrm{inst}} = 10^{32} \frac{1}{\mathrm{cm}^2 \mathrm{s}}$, and will be increased soon to $10^{33} \frac{1}{\mathrm{cm}^2 \mathrm{s}}$ and $10^{34} \frac{1}{\mathrm{cm}^2 \mathrm{s}}$. Each luminosity will require proper energy thresholds corresponding to the desired task.

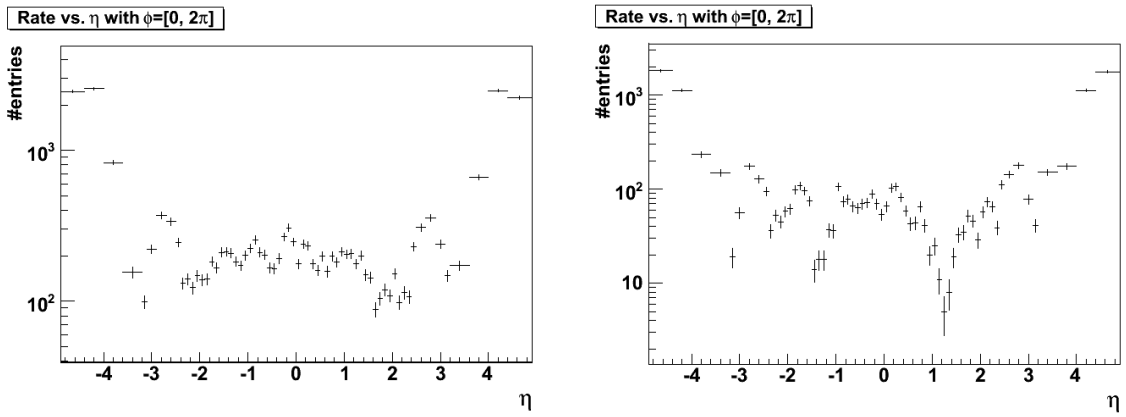


(a) Electromagnetic Calorimeter.



(b) Hadronic Calorimeter.

Figure 4.10: Dependency of rates as a function of the energy threshold $E_{\mathrm{T,\,thresh}}$ for the central region $\eta = [-1.6, 1.6]$, $\phi = [0, 2\pi]$. The rates are normalised on 0.1×0.1 in $\Delta\eta \times \Delta\phi$. As expected from (4.1), the rate has the shape $\sim E^{-4}$. The drop at energies above $\sim 160\,\mathrm{GeV}$ is due to insufficient statistics (see table 4.1).



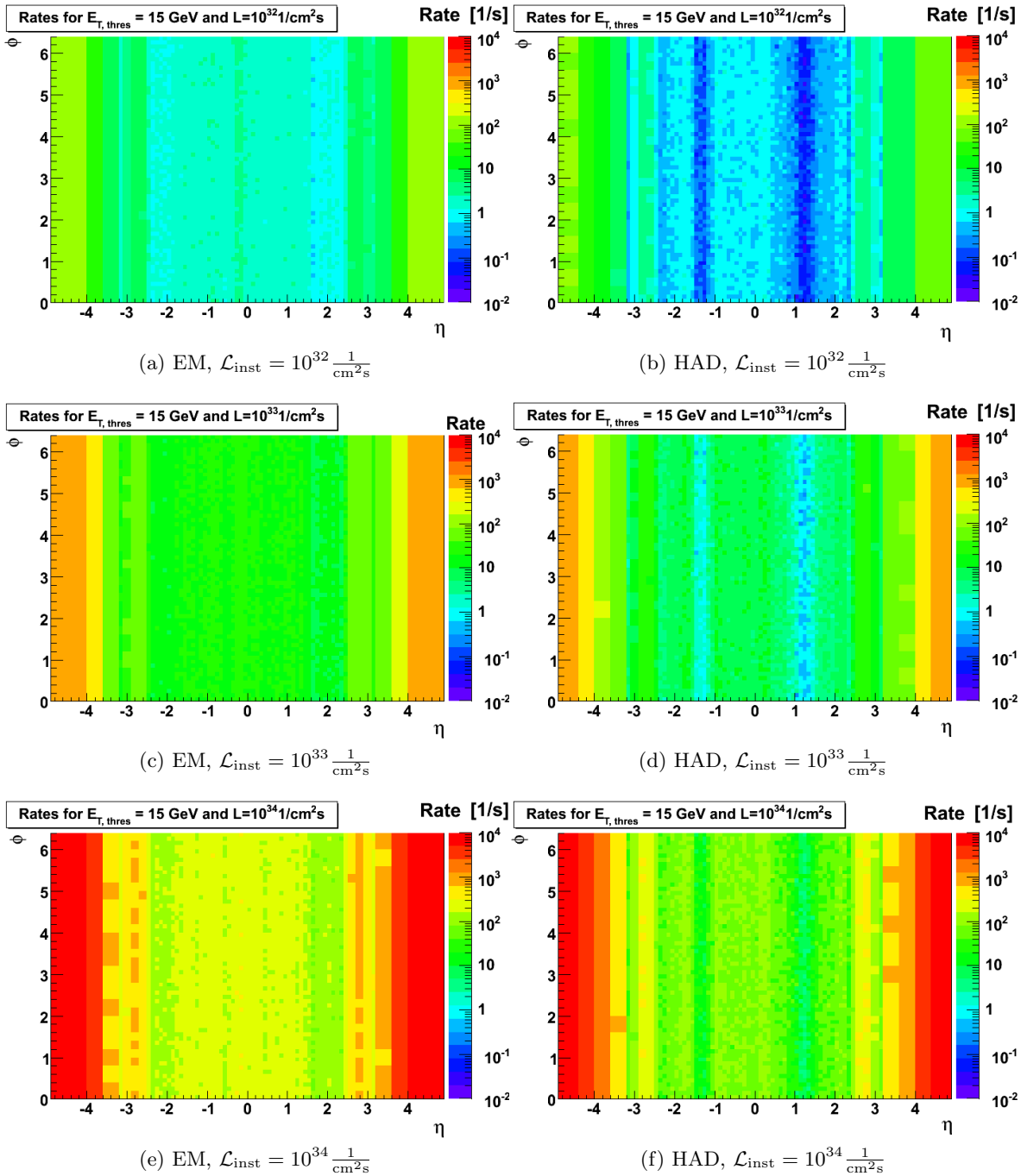
(a) EM (b) HAD

Figure 4.11: Rate distribution for $-4.9 < \eta < 4.9$ as an average over ϕ for $E_{\mathrm{T,\,thresh}} = 15\,\mathrm{GeV}$, $\mathcal{L}_{\mathrm{inst}} = 10^{34} \frac{1}{\mathrm{cm}^2\mathrm{s}}$ and $t = 1\,\mathrm{s}$.

2. The choice of the energy threshold also depends on the physics situation and the intention of the monitoring. Low energy thresholds (e.g. 2 GeV) will be strongly affected by electronic noise, thus are useful for diagnostic purposes, but inappropriate for calibration procedures.

The development of the rates with increasing luminosity is shown in figure 4.12 by the 2-dimensional histograms of the rates in the η-ϕ plane for a threshold energy of $E_{\mathrm{T,\,thresh}} = 15\,\mathrm{GeV}$. Since FCAL2 and FCAL3 of the hadronic calorimeters are staggered in depth but cover the same area, they are placed side by side: FCAL2 is displayed from $3.2 < |\eta| < 4.0$ and FCAL3 from $4.0 < |\eta| < 4.9$, both with squeezed size in η by a factor of 1/2.
The histograms contain the rate as an average over time in units of [1/s]. In order to obtain the rates in a finite time interval as expected at the experiment, i.e. discrete rate counts, the histograms are used as a basis for further simulations. It consists of randomly filling a new histogram N-times based on the contents of the existing histogram, which results in a *realistic* poisson distribution of the rates. N depends on the total rate at the specific energy threshold as well as the time interval t during which the rates are counted. All following plots are obtained with the described method.
Figure 4.11 shows the rate as a function of η for a time interval of one second and a luminosity of $\mathcal{L}_{\mathrm{inst}} = 10^{32} \frac{1}{\mathrm{cm}^2\mathrm{s}}$. The entries are an average over ϕ, normalised to their nominal bin size in η-ϕ. The trigger towers in the end-cap and forward region cover a larger area: mainly a factor of 4 for the end-cap and a factor of 16 for the forward region (see figure 3.4). Because of this inhomogeneous granularity, an individual energy threshold related to the size of the TT and according to the dependency of rates on the threshold as stated in figure 4.10 should be considered. Since the forward region is furthermore hardly penetrated by minimum bias events, it is also conceivable to adjust the thresholds in general with the pseudorapidity η. This finally depends on the desired purpose and the object of interest.

Aside, the figure reveals the structure of the calorimetry (compare figure 2.4). Although not fully understood, at least in the transition region from the electromagnetic end-cap to the forward calorimeters ($\eta = 3.2$), a crack in the η-acceptance is noticeable. The effect of cracks and dead material is even more drastically observable in the hadronic data. The transition



(a) EM, $\mathcal{L}_{\text{inst}} = 10^{32} \frac{1}{\text{cm}^2\text{s}}$

(b) HAD, $\mathcal{L}_{\text{inst}} = 10^{32} \frac{1}{\text{cm}^2\text{s}}$

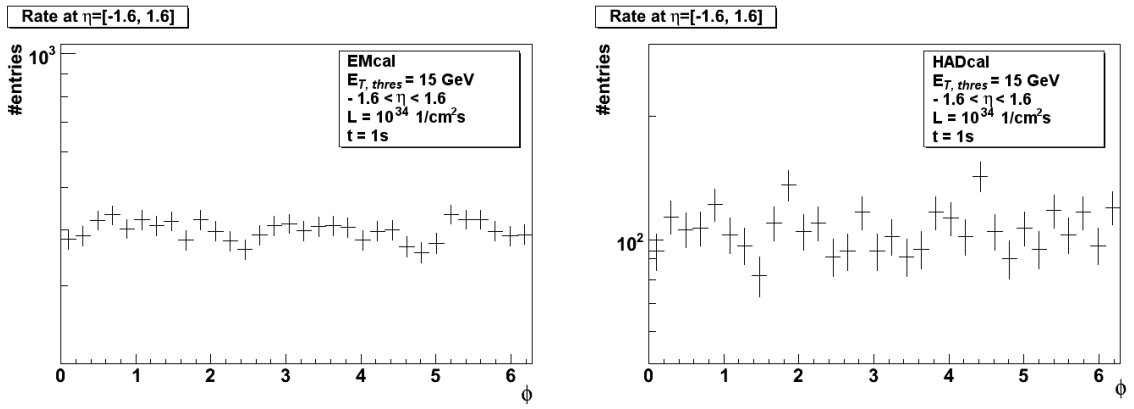
(c) EM, $\mathcal{L}_{\text{inst}} = 10^{33} \frac{1}{\text{cm}^2\text{s}}$

(d) HAD, $\mathcal{L}_{\text{inst}} = 10^{33} \frac{1}{\text{cm}^2\text{s}}$

(e) EM, $\mathcal{L}_{\text{inst}} = 10^{34} \frac{1}{\text{cm}^2\text{s}}$

(f) HAD, $\mathcal{L}_{\text{inst}} = 10^{34} \frac{1}{\text{cm}^2\text{s}}$

Figure 4.12: Rate for an energy threshold of $E_{\text{T, thresh}} = 15\,\text{GeV}$ at different luminosities.



(a) EM (b) HAD

Figure 4.13: Rate distribution for $0 < \phi < 2\pi$ for the central region $-1.6 < \eta < 1.6$ and $E_{\mathrm{T,\ thresh}} = 15\,\mathrm{GeV}$, $\mathcal{L}_{\mathrm{inst}} = 10^{32}\,\frac{1}{\mathrm{cm^2 s}}$, $t = 1\,\mathrm{s}$.

luminosity $[\frac{1}{\mathrm{cm^2 s}}]$	$E_{\mathrm{T,\ thresh}}$ [GeV]	#events per bin EM	HAD
10^{32}	5	~ 150	~ 40
10^{33}	10	~ 300	~ 40
10^{34}	15	~ 300	~ 100

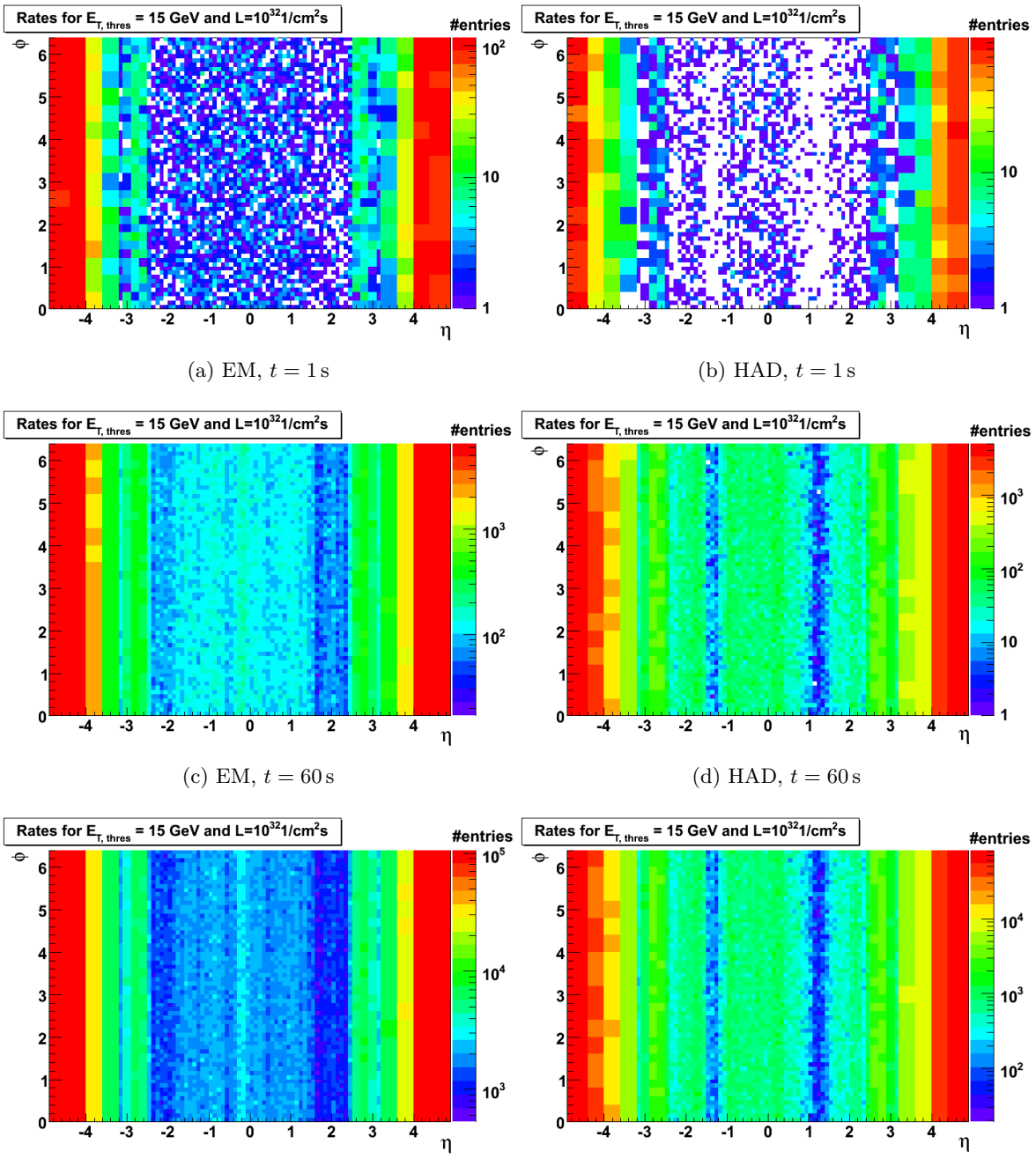
Table 4.3: Energy thresholds considered for further analysis. The number of events is related to the central region $\eta = [-1.6, 1.6]$, $\phi = [0, 2\pi]$.

region between barrel and the extended barrel ($0.8 < |\eta| < 1.3$) contains a considerable amount of support structure, which apparently absorbs a large fraction of hadronic particles. Moreover, a slight asymmetry in η was observable for all distributions. Whether this is a statistical or systematical effect is not fully understood [24] and should be part of further analysis.

The distribution in ϕ is shown in figure 4.13 for the central region $-1.6 < \eta < 1.6$. Due to the applied smoothing, it is basically flat in ϕ showing only statistical fluctuations as expected.

For a low luminosity, the time interval t has to be extended in order to achieve satisfactory statistics. Of course, this finally depends on the desired purpose: In case of e.g. calibration purposes, the required rate count would be in the order of 10^3 [23], so that $t_{\mathrm{req}} = 1\,000\,\mathrm{s}$ for the hadronic calorimeter, since the rate is approximately 1 Hz. Figure 4.14 shows the rate maps for time intervals of 1 s, 60 s and 1 000 s and a luminosity of $\mathcal{L}_{\mathrm{inst}} = 10^{32}\,\frac{1}{\mathrm{cm^2 s}}$.

The monitoring of the detector activity in real-time would require a relatively high rate of at least 100 Hz for a minimum refresh frequency of 1 frame/s. This is only achievable with lower thresholds. From 4.10, three thresholds seem to be considerable after all: 5 GeV, 10 GeV and 15 GeV. These cover low luminosity scenarios with the monitoring of dead or faulty channels in real-time as well as high luminosity scenarios, where the focus is on e.g. the beam quality. Table 4.3 shows the approximated rates corresponding to the three thresholds, and figure 4.15 the respective 2-dimensional rate histograms.



(a) EM, $t = 1\,\mathrm{s}$

(b) HAD, $t = 1\,\mathrm{s}$

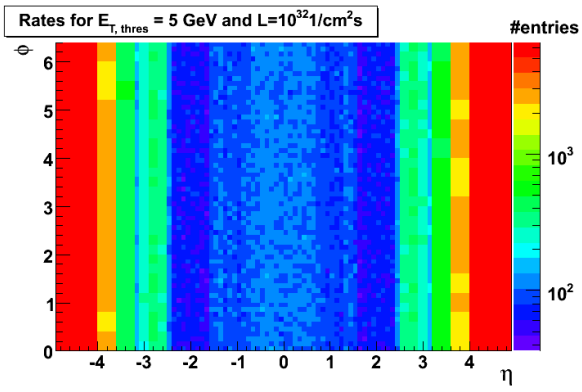
(c) EM, $t = 60\,\mathrm{s}$

(d) HAD, $t = 60\,\mathrm{s}$

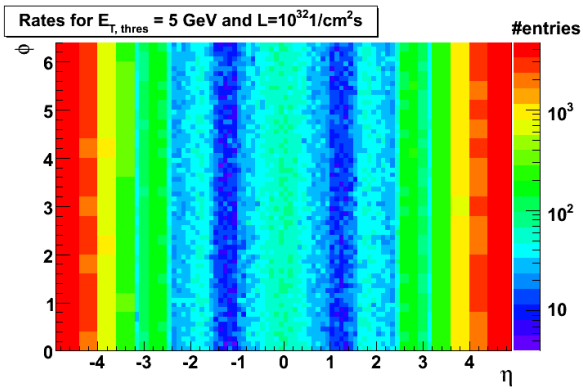
(e) EM, $t = 1\,000\,\mathrm{s}$

(f) HAD, $t = 1\,000\,\mathrm{s}$

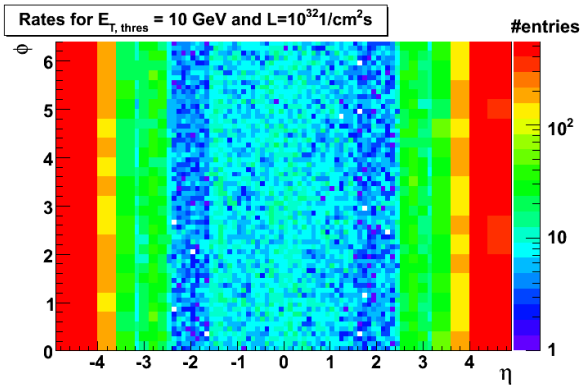
Figure 4.14: 2-dimensional map containing the rate counts at $E_{\mathrm{T,\,thresh}} = 15\,\mathrm{GeV}$, $\mathcal{L}_{\mathrm{inst}} = 10^{32}\,\frac{1}{\mathrm{cm}^2\mathrm{s}}$ for various time intervals t.



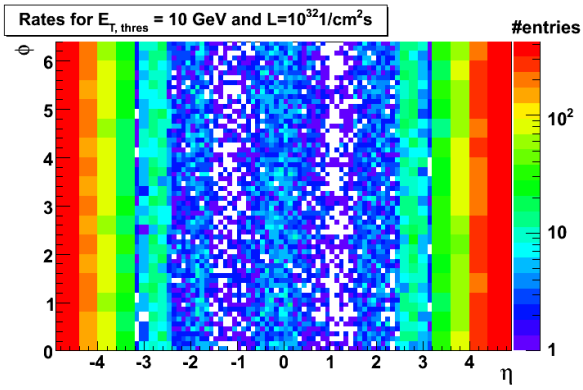
(a) EM, $E_{\mathrm{T,\ thresh}} = 5\,\mathrm{GeV}$



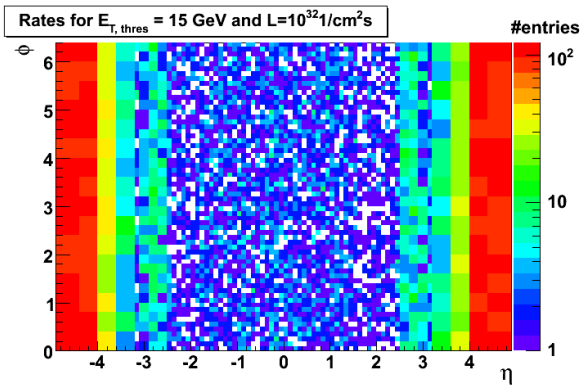
(b) HAD, $E_{\mathrm{T,\ thresh}} = 5\,\mathrm{GeV}$



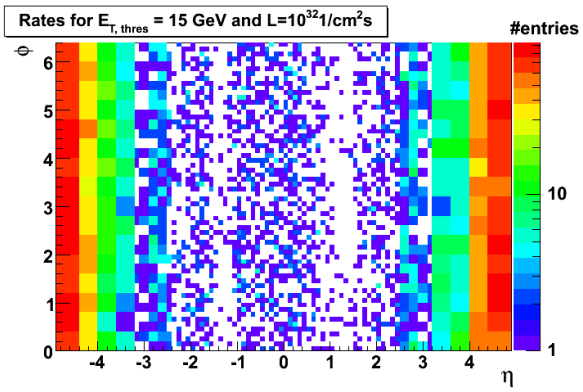
(c) EM, $E_{\mathrm{T,\ thresh}} = 10\,\mathrm{GeV}$



(d) HAD, $E_{\mathrm{T,\ thresh}} = 10\,\mathrm{GeV}$



(e) EM, $E_{\mathrm{T,\ thresh}} = 15\,\mathrm{GeV}$



(f) HAD, $E_{\mathrm{T,\ thresh}} = 15\,\mathrm{GeV}$

Figure 4.15: Rate map for a luminosity of $\mathcal{L}_{\mathrm{inst}} = 10^{32}\frac{1}{\mathrm{cm}^2\mathrm{s}}$, $t = 1\,\mathrm{s}$ and various threshold energies $E_{\mathrm{T,\ thresh}}$.

4.5 Conclusions

The dependency of the rates was studied systematically as a function of the detector luminosity, different threshold energies and various time intervals. A threshold energy in between 5 GeV and 15 GeV seems to be reasonable and allows a variation in the rate counts of a factor of about 100. At low luminosity of $\mathcal{L}_{\text{inst}} = 10^{32} \frac{1}{\text{cm}^2\text{s}}$ in the early stage of the LHC, a threshold of $E_{\text{T, thresh}} = 5\,\text{GeV}$ in combination with a frequent readout of 1 Hz should be considered for diagnostic purposes. With increasing luminosity and a reliable system, higher thresholds in the order of 15 GeV become interesting for long-term studies like e.g. calibration tasks.
In terms of using the Rate Metering as a monitor of beam parameters, the impact of beam shift and beam halo on the rates should be part of further investigation.

Chapter 5

Rate Metering Test Setup

The Rate Metering and Histogramming functionality of the PPM cannot be tested with onboard methods. Therefore, a test setup in a fully controlled laboratory environment had to be developed which emulates the calorimeter signals externally and provides them in the form they are transmitted to the PPM in the final system. This test setup must comply with the following requirements:

- Analogue signals with well defined shape, timing and amplitude have to be provided in order to test the rate metering, including a test of the analogue signal processing chain as implemented on the AnIn board and the FADC on the PPM.
- A multi-channel source is required for a thorough testing of all channels of a PPM in parallel.
- Synchronisation not only within all signals themselves but also to the 40 MHz bunch crossing frequency, which is commonly used as clock for the whole Level-1 Calorimeter Trigger System and has to be provided for the test setup as well.

The three tasks are covered by the concept illustrated in the block diagram in figure 5.1. The basic idea is to use the output of a commercial graphics card as source for single-ended analogue signals. The output signal is then processed by the so-called Fan-out and Amplification Board (FAB) with a fan-out and a conversion to differential signals with voltage levels adequate for the PPM input. Moreover, an additional device is built which generates a stable clock synchronous to the signals of the graphics card using one of the channels as reference.

5.1 Signal Generation with a Graphics Card

It will be shown that a commercial graphics card is a cheap and likewise appropriate alternative to an arbitrary signal generator in terms of time resolution, resolution in amplitude, signal quality, handling and generation of multiple signals.
The key parameters of the signal generator are given by the properties of the pulses to be emulated as described in chapter 3.2.1. Summarising, these are a rise time of approximately 50 ns and an amplitude of $U_{\max} = 2.5\,\mathrm{V}$, which is followed by an undershoot with $U \approx 0.5\,\mathrm{V}$ and a total length of $\sim 450\,\mathrm{ns}$ in the case of the LAr calorimeters.
However, for the following discussion of the graphics card properties, the exact values of the voltage ranges are less important; they will be corrected for at a later point, including a

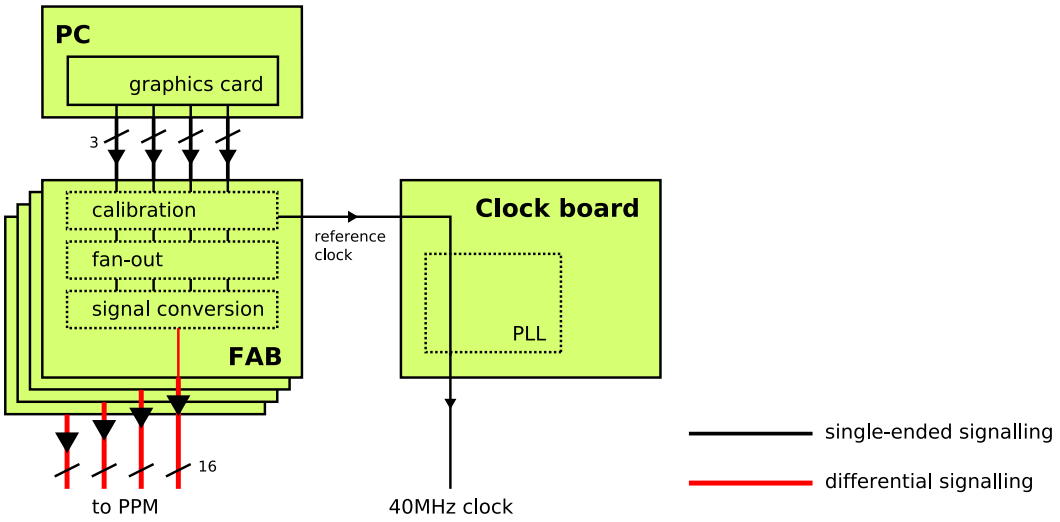


Figure 5.1: Block diagram of the test setup. The input is generated by a graphics card and then transformed into a differential signal by the so-called fan-out and amplification board (FAB). In parallel, a 40 MHz clock is derived which can be provided to the the PPM.

conversion to a differential signal. The focus is moreover on the general shape of the pulse in terms of the resolution of amplitude and timing.

An analogue monitor output of a graphics card basically consists of three signal channels, used for the colours red, green and blue, and two signals for synchronisation purposes (HSYNC, VSYNC). The output voltages of the *colour signals* lie within a range of approximately 0 V to 0.7 V and correspond to the brightness of that colour. A common colour depth of 24-bit therefore means that a 8-bit value is mapped to a 0.7 V range. The images then contain three independent signals at once (red, green and blue) and the pulse amplitude represents the brightness of each colour. Though the output only has discrete voltage levels, the achieved voltage resolution of $\sim 0.4\%$ of the output signal and the corresponding step size of $\Delta U_{\text{out}} = 2.73\,\text{mV}$ is small enough to emulate calorimeter pulses. Furthermore, it will be shown that the output is very precise concerning linearity.
The time resolution depends on the maximum frequency that the graphics card can change colours with. This is, in terms of graphics, the interval between two pixels and is called *PIXELCLOCK*. Typical values are in between 160 MHz (6.25 ns) and 200 MHz (5 ns). That is in good compliance with the requirement of sampling pulses with a rise time of 50 ns (3.2.1), since the eight bins in the case of e.g. $\Delta t = 6.25\,\text{ns}$ would be satisfactory to simulate the edge of the pulse.
Concluding, the output signal of the graphics card with its small step size of the digital output voltage and the good time resolution can be treated as analogue and is very suitable to simulate the shape of calorimeter pulses.

The graphics card creates the screen by successively displaying the pixels line by line starting in the top left corner. At the end of each line, a blanking space with fixed number of black pixels is induced for the horizontal synchronisation (HSYNC). This originates in the

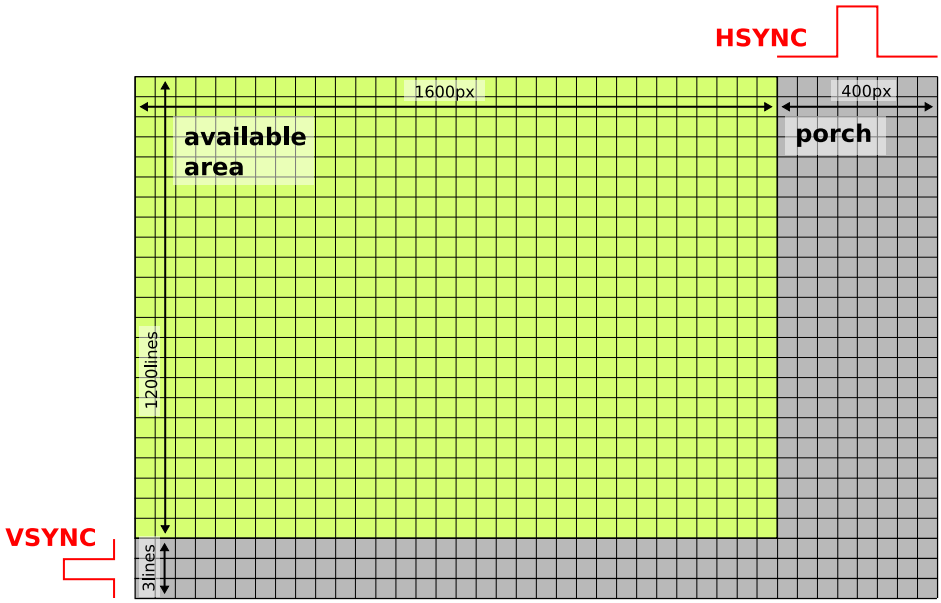


Figure 5.2: Illustration of the screen proportions. The visible area is framed by a so-called *porch*, which covers about 20% of the total screen and where no signal can be set. Within the porch, the synchronisation pulses HSYNC and VSYNC are sent.

electron beam technique of CRT[1] monitors that need time to reset the beam deflection magnets in order to start at the next line. During that interval, the electron beam is switched off, and therefore no signal is generated by the graphics card, too. In the same way, the vertical synchronisation (VSYNC) after completion of the image results in several lines of black pixels. The effect of that so-called *porch* is that about 20% of the physical signal is unavailable for signal generation.
This restriction turns out not to be very serious if one considers that on the one hand the blanking space from the signal generator would be interpreted by the PPM as a calm calorimeter (thus does not interfere) and on the other hand the maximal length of calorimeter pulses including undershoot is in the order of $t_{\text{pulse}} = 500\,\text{ns}$. Assuming for example a moderate PIXELCLOCK of $f_{\text{pixel}} = 160\,\text{MHz}$ and a visible screen resolution of $1600 \times 1200\,\text{px}$ with a physical resolution of $2000 \times 1203\,\text{px}$ including porch (see figure 5.2). Hence, the largest continuous sequence of pixels is one line with a corresponding time interval of $1600\,\text{px} \cdot 6.25\,\text{ns} = 10\,\mu\text{s}$, i.e. about 20 pulses fit into it. In total, 24 000 pulses can be displayed per screen, as

$$t_{\text{visible}} = \frac{1600 \cdot 1200}{f_{\text{pixel}}} = 12\,\text{ms}.$$

This is considered to be satisfactory space to vary pulse shapes, which means that displaying fixed images is sufficient. The maximum and minimum rates that pulses can be generated with are

$$f_{\text{max}} = f_{\text{pixel}} \frac{20 \cdot 1200}{2000 \cdot 1203} = 1.60\,\text{MHz}$$

$$f_{\text{min}} = f_{\text{pixel}} \frac{1}{2000 \cdot 1203} = 66.5\,\text{Hz}.$$

[1] CRT - cathode ray tube.

In order to achieve lower rates, real-time graphic memory writing would be needed, but is not considered necessary at this point.

It was mentioned already that the voltage range of the graphics card output does not comply with the voltage levels of the calorimeter pulse to be simulated. Since the output of the graphics card is unipolar, i.e. the output voltage is strictly positive, it is even inappropriate to generate the required negative signals for the LAr undershoot. This drawback is addressed by a subsequent device that is introduced in section 5.3. It includes both a mapping of the output voltage range to the adequate values and a base line shift of the graphics card output to negative voltages. Of course, the latter statements on the appropriateness of the graphics card properties are valid nevertheless.

Graphics Card Inter-Synchronisation and Synchronisation to Bunch Crossing Frequency

Graphics cards nowadays feature up to four monitor outputs, so-called 4-HEAD or QUAD-HEAD[2] graphics cards, with $4 \cdot 3 = 12$ independent colour channels. For the creation of multiple independent signals beyond the number of channels on a single graphics card, several graphics cards have to be combined. The challenge is then to synchronise all outputs not only between themselves (PIXELCLOCK, HSYNC resp. VSYNC) but also to a 40 MHz clock (bunch crossing frequency) that is necessary as input reference for the PPM. Both requirements are equivalent: Either the graphics card inter-synchronisation is based on a master clock[3], which can also be the source of the 40 MHz clock. Or, supposing the inter-synchronisation is existent[4], one of the various channels available is used to generate a 40 MHz clock signal directly.

Commercial Solutions

Only very few systems for graphics card inter-synchronisation are on the market, which are intended for large-sized data walls, multi-monitor vehicle simulation (pilot training), video technology or distributed rendering to balance scene complexity across multiple systems and display controllers. Currently, only nVidia's *Quadro G-Sync* system [26] is commercially available, but was not considered due to its price.
On request, Matrox offered its *Advanced Synchronisation Module* (ASM) for testing purposes[5]. It is capable of synchronising up to four Matrox display controllers in one PC to an external reference frequency (the so-called *house sync*), as well as synchronising multiple systems equipped with the Matrox ASM and supported Matrox display controllers among themselves using a master / slave configuration [27].

The system was tested concerning synchronisation to an external clock with a single Matrox QID Pro graphics card as target display controller as shown similarly in figure 5.3. The external clock is generated by a signal generator and provided to the ASM as reference frequency via the house sync input. It has to be of the order of the vertical refresh rate

[2]The term *HEAD* will be used throughout this thesis synonymically for monitor outputs.
[3]This is often referred to as *genlock* (nVIDIA) [25] or *house-sync* (MATROX) and used in video technology.
[4]So-called *frame lock* systems.
[5]The product is not freely available on the market as it does not suite the Matrox quality standards. Nevertheless Wolfgang Bichlmeier, OEM Sales Manager at Matrox Electronic Systems GmbH in Munich, Germany, kindly offered a sample for testing purposes.

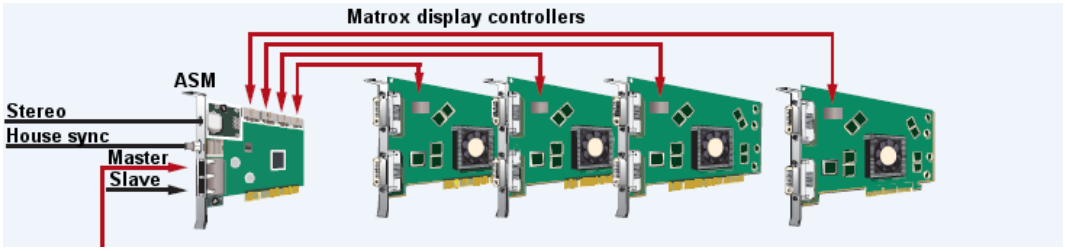


Figure 5.3: Matrox *Advanced Synchronisation Module* (ASM) in combination with several Matrox QID graphics cards (from [27]).

(VSYNC) of the graphics card, i.e. $\sim 60\,\text{Hz}$. A link from the ASM to the QID Pro manages the control of the horizontal and vertical synchronisation of the graphics card.

The synchronisation process is based on the continuous phase comparison of the VSYNC signal of the graphics card and the reference frequency. First, the ASM sets the VSYNC frequency f_{QID} of the target display controller close to the reference frequency, but systematically below $f_{\text{ref}} = f_{\text{ASM}}$, with $\Delta f \approx 1\,\text{kHz}$. This has the effect that the phase of the reference signal and the VSYNC signal continuously changes, in fact until the phase difference between them is basically zero at a point. When this happens, the ASM applies a fixed-sized phase correction to the display controllers in the opposite direction. This *push back operation* is of the order of microseconds and occurs repetitively. Figure 5.4 illustrates the process. Concluding, the synchronisation process with the ASM is associated with unavoidable overall jitter in the range of μs, which is well suitable for video applications, but insufficient for our case, where precision down to 1-2 ns is needed. Hence, the tested commercial solution is inadequate for synchronisation at the required precision.

Nevertheless, the Matrox QID Pro being a 4-HEAD system is very suitable to act as a 12 channel signal generator as a minimum solution and is discussed in section 5.1.

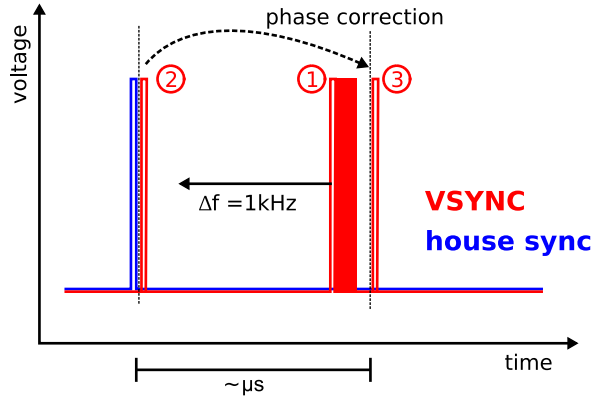


Figure 5.4: Synchronisation procedure of the Advanced Synchronisation Module. (1) The frequencies of the ASM $f_{\text{house sync}}$ and the graphics card f_{VSYNC} differ slightly. Hence, the phase difference between the reference signal (blue pulse, left side) and the VSYNC signal (red pulse) continuously changes. Once reaching a certain limit (2), the ASM applies a fixed-size phase correction in the range of μs (3). This causes continuous jitter among the two frequencies.

Custom Solutions

Apart from the commercial solution, the synchronisation of several graphics cards by minor modifications of the cards is an option. The ideal target board would be a simple graphics card with basic 2D features and an easy accessible clock chip. The GPU[6] should be robust on minor frequency variations, so that an external PLL[7] could replace the graphics card's clock and realise synchronisation between several cards.
This approach was investigated on the basis of several graphics cards, of which the Matrox Millenium G400 is discussed in the following as representative example.

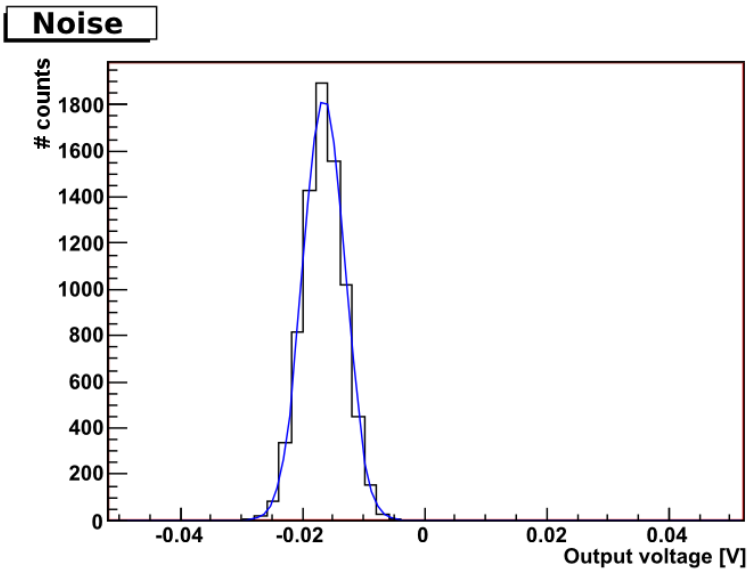


Figure 5.5: Noise of the Matrox G400 (HEAD1, blue channel). Noise was measured by setting all pixels to black. A gaussian fit results in $\mathrm{RMS}_{\mathrm{blue}} = 3.4\,\mathrm{mV}$. Obviously, the baseline of the output differs from 0. This is observed on all tested graphics cards (deviations of up to $20\,\mathrm{mV} \approxeq 3\%\ U_{\mathrm{max}}$) and requires correction.

Matrox Millenium G400

The Matrox Millenium G400 was used in former tests of the AnIn boards and is part of the MCM test setup [17], though only one of its two monitor outputs is used.
The card is capable of resolutions up to $1920 \times 1200\,\mathrm{px}$ at a PIXELCOCK of 200 MHz, hence a 50 ns rise time is sampled by 10 bins. Linearity, noise and crosstalk were measured using the data recording function of a tektronix oscilloscope. Therefore, images of constant brightness were displayed with the graphics card at a screen resolution of $1600 \times 940\,\mathrm{px}$ at a PIXELCLOCK of 200MHz. Since the output voltage of the graphics card is zero at the blanking space, the measurement takes into account single lines of the image by taking data in a gated time interval of 7.8 µs. The tektronix oscilloscope has a data acquisition rate of 10^9 samples per second, hence 7 800 data points were stored. The mean and the error margins of each data set were calculated using a gaussian fit of the voltage level distribution, at which

[6] GPU - graphics processing unit.
[7] PLL - Phase-Locked Loop; PLLs are discussed in detail in section 5.4.2.

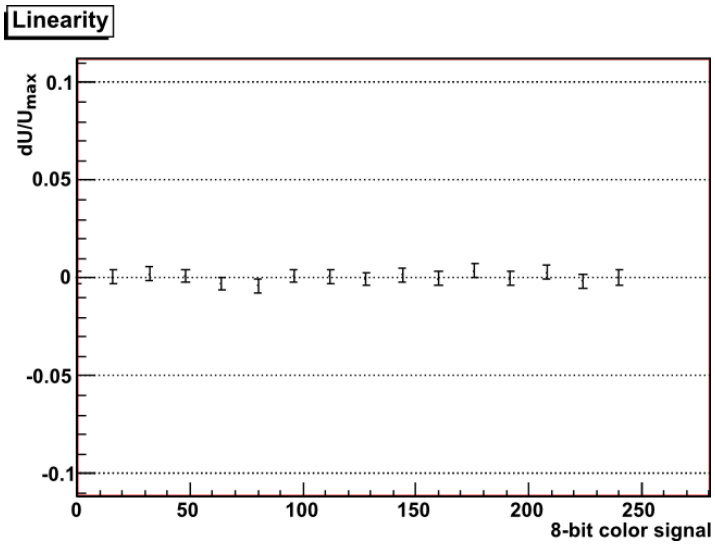


Figure 5.6: Linearity of the Matrox G400 (HEAD1, blue channel). The ordinate is the residual of measured values and the fitted curve. All values are within 1 %.

the RMS[8] was used as error margin. By measuring the output voltage while a black image is displayed, the average noise has been determined as $\mathrm{RMS}_{\mathrm{noise}} = (3.46 \pm 0.05)\mathrm{mV}$, which lies within the noise level of the oscilloscope (see figure 5.5). It occurred that the baseline of the output differs from zero. This has to be taken into account when the graphics card output is mapped to the final voltage range at a later stage of the signal chain (see section 5.3.3).

The linearity was estimated using 17 different images with brightness levels of 0, 16, 32, ..., 255 in order to cover the full 8-bit range. Every brightness level provides one data point, and a linear fit was performed. The result is shown in figure 5.6 as the residual of the output voltage (normalised to the maximum output voltage) versus the digital 8-bit brightness value of the graphics card. All values are within 1%.

Crosstalk was estimated such that one channel acts as realistic crosstalk source by applying a 40MHz clock signal. Neighbouring channels showed a distinguishable crosstalk signal and the noise RMS of the affected channel is fairly doubled. This problem was found similarly for all graphics cards tested and turned out to be the dominant noise source.

The graphics card features two monitor outputs, a so-called DUAL-HEAD configuration. The relative phase of the output was measured by comparing the synchronisation pulses VSYNC_1 and VSYNC_2. The fact that only one clock chip was identified on the card should lead to synchronous timing of the two outputs as they are deduced from the same reference clock. Figure 5.7 shows that this is not true, rather their vertical refresh rates differ with about 0.5 Hz. Therefore, the card is not an option as multi-channel signal source.

Other cards were considered and tested, but proved to be inappropriate rather because of the complexity of the board (Matrox QID Pro) or missing drivers (ATI FireMV 2400)[9].

[8] RMS - root mean squared.

[9] With the long-awaited publication of the source code of its drivers, ATI currently forced the development of 3rd party drivers for linux systems, which should be available soon and allow for an attempt with this very promising graphics card.

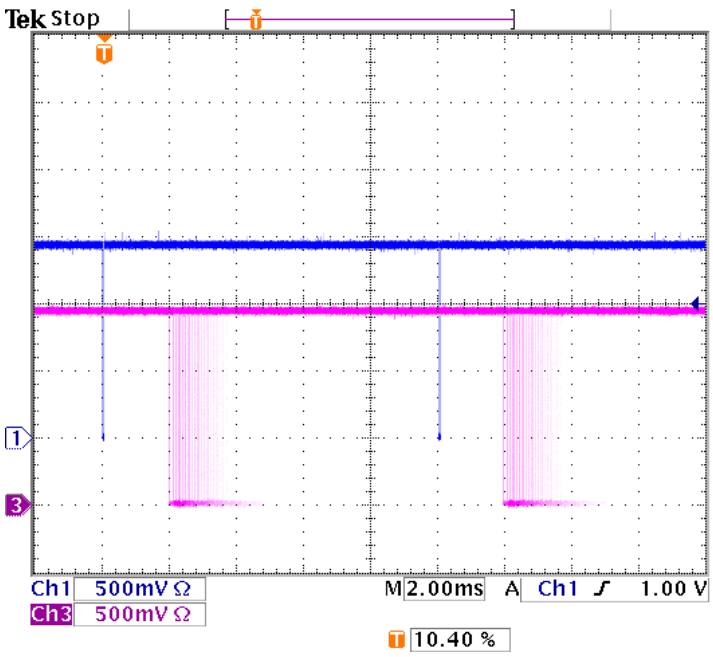


Figure 5.7: Synchronicity of the two HEADs of the Matrox G400: Although the outputs are derived from the same clock, the VSYNC signals of HEAD1 (CH1) and HEAD2 (CH3) differ with about 0.5 Hz.

Matrox QID Pro

The Matrox QID Pro is a graphics card for a 64-bit PCI slot and supports up to four monitor outputs (QUAD-HEAD). The relevant technical constraints are summarised in table 5.1.

A single graphics chip based on the Matrox' Parhelia series controls all four displays. However, HEAD1 and HEAD2 on one side and HEAD3 and HEAD4 on the other side showed a similar behaviour with respect to driver configuration and synchronisation. Physically, their signals are split on two LFH60 connectors at the slot bracket, each containing the signals of two outputs. The used linux driver (see A.1) only permits a wide screen configuration that combines the two screens of the same connector. Furthermore, HEAD3 and HEAD4 differ from HEAD1 and HEAD2 with respect to the vertical synchronisation such that the signals are shifted in time with $\Delta t = 12.5\,\mu s$, which equals exactly one line (see figure 5.8). This has to be taken into account by the software as described in section 5.2.
Additionally, a stable, but non-zero phase between the graphics card's HEADs is observed. It varies within about 2 ns for every initialisation of the driver of the graphics card. As this phase shift is unavoidable, it defines the minimal accuracy of the synchronisation of the signals. Linearity, noise and crosstalk have been measured. The left side of figure 5.9 shows the pattern that was used to estimate the linearity. It consists of 17 lines each with constant brightness values (0, 16, 32, ..., 255). The mean voltage of each line is measured using the oscilloscope measuring functions (figure 5.9, right side) and gives one data point (mean voltage, brightness), on which a linear fit is performed. The result is shown in figure 5.10 as the difference of the fitted curve and the data points. All points are within a 1% range and agree with zero within the uncertainties, estimated from RMS noise (3.89 ± 0.14) mV. Moreover, the crosstalk significantly affects neighbouring channels as shown in figure 5.11,

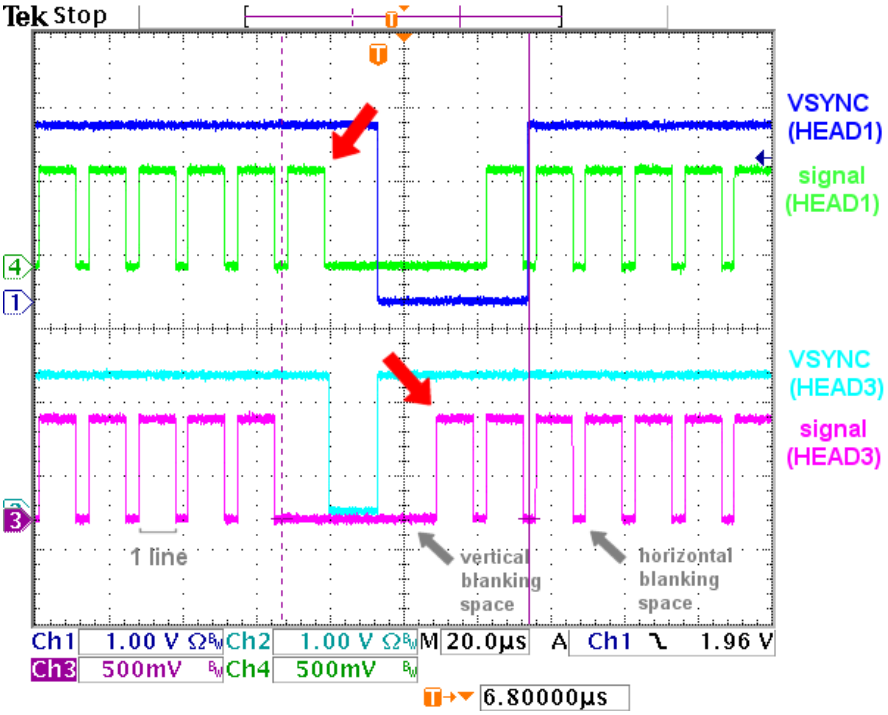


Figure 5.8: Blanking space at the vertical synchronisation for HEAD1 (CH1: VSYNC, CH4: signal) and HEAD3 (CH2: VSYNC, CH3: signal). As test pattern for the signal channels, the maximum output signal was chosen (255 → 700 mV). HEAD1 shows improper behaviour concerning the VSYNC pulse (the pulse should lie within blanking space) and the signal is delayed by one line plus blanking space.

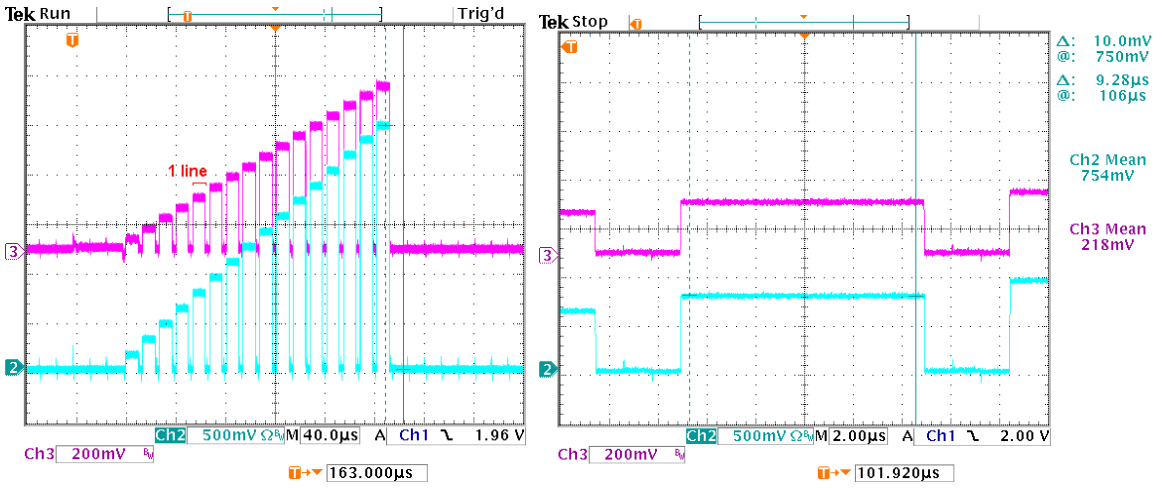


Figure 5.9: Oscilloscope picture that shows the pattern (left) to measure linearity of the analogue signal at the graphics card output (CH2, cyan). The pink signal, CH3, was measured at a subsequent stage of the signal processing chain and is discussed in section 5.3.4. Every *step* corresponds to 1600 px = 1 line with a constant voltage level. The figure on the right shows one line, of which the mean value is measured in the interval marked by the cursors of the oscilloscope. With the resulting data points, the linearity is estimated (see figure 5.10).

where a 40 MHz clock signal was applied to one channel while measuring another channel from the same HEAD, which carries a constant signal.

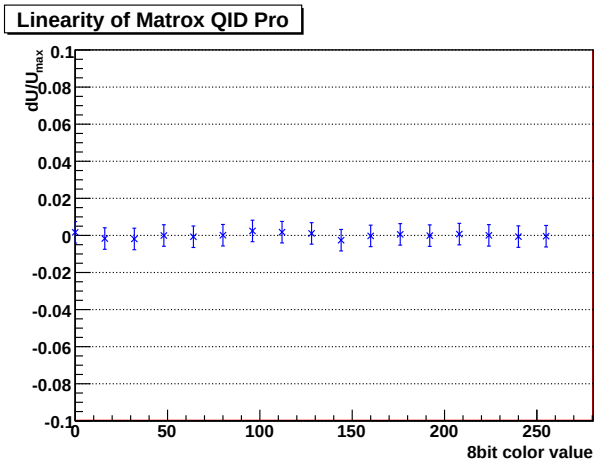


Figure 5.10: Linearity of the Matrox QID Pro. All values are within 1%.

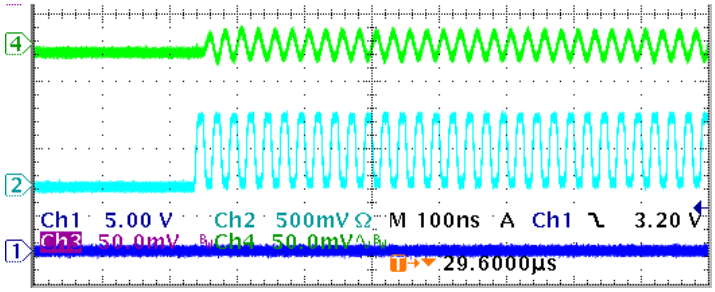


Figure 5.11: Crosstalk at the graphics card output. Channel 2 (cyan) carries a 40 MHz clock signal, which significantly affects the neighbouring channel (CH4, green).

Summary

The properties of a graphics card signal satisfactorily comply with the requirements to simulate a calorimeter pulse concerning time and amplitude resolution. Most critical are the influence of crosstalk between channels, which is nevertheless within the acceptable limits, and the phase difference between the HEADs. The Matrox QID Pro stands out as appropriate graphics card due to its good electrical properties, the number of featured channels and the acceptable synchronicity between them.
Inter-synchronisation of graphics cards could not be achieved at this point, but is object of further investigation and still considered in all the following steps.

	Matrox G400	Matrox QID Pro	ATI FireMV 2400
HEADS	2	4	4
Channels	6	12	12
Synchronicity	-	$\sim$ 2ns (const)	N/A
Maximum PIXELCLOCK	200MHz	160MHz	N/A
Maximum resolution	1920×1200px	1600×1200px	N/A
Maximum voltage	540mV	670mV	N/A
RMS noise	3.46mV	3.89mV	N/A
Linux driver support	✓	✓[10]	-[11]

Table 5.1: Overview of the graphics cards considered for inter-synchronisation.

5.2 Data Preparation and Software

The foremost advantage apart from the multiplicity of channels of the graphics cards as signal generator is the flexible programming of the output. In order to summarise the required features of the dedicated software, the template signal pulses are described before. Furthermore, the physical constraints inherited from the graphics card are taken into account.

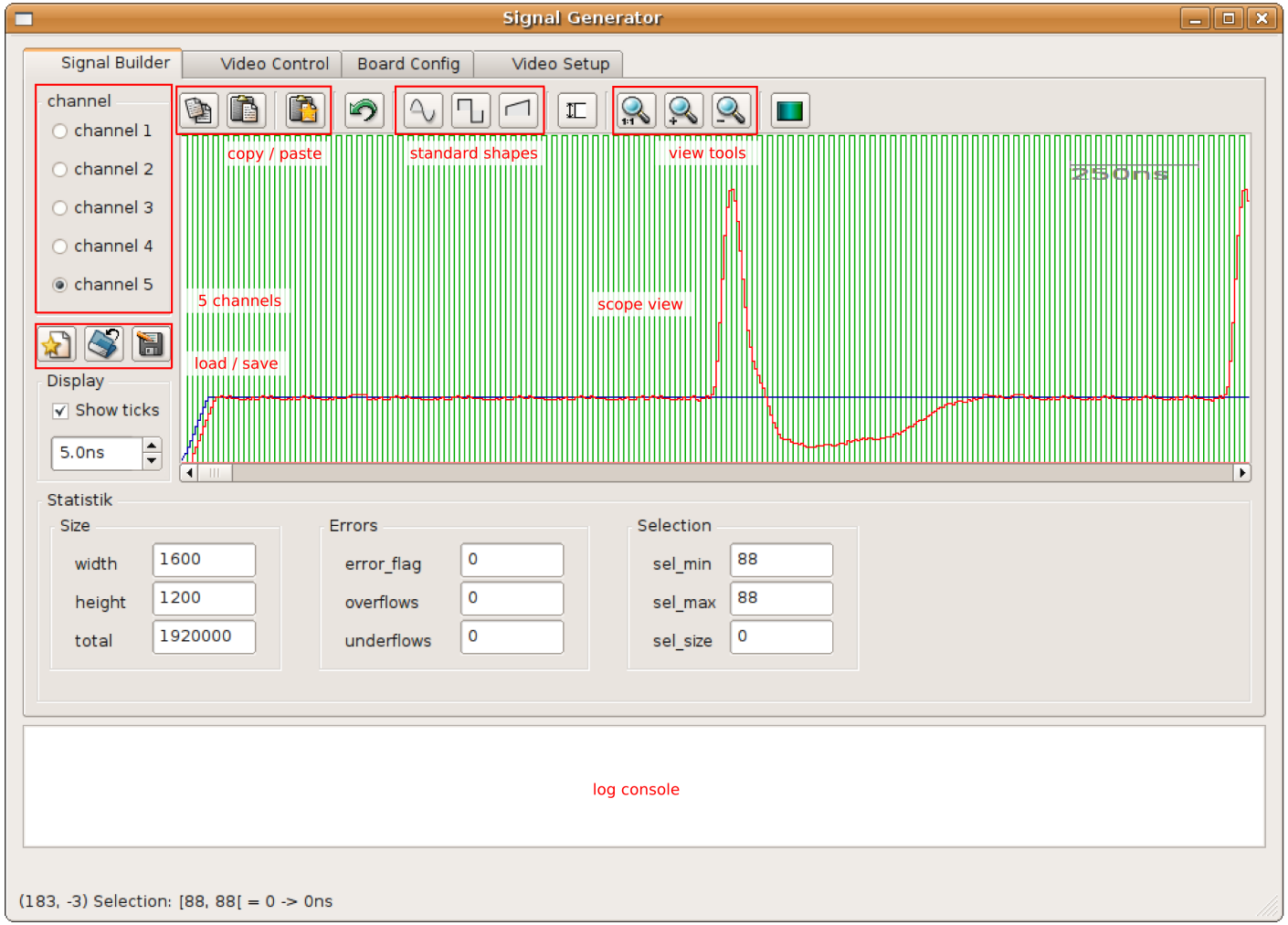
Data format. The data is taken from the *Trigger Tower Analogue Signal Library* (TITAN) [28], which consists of pulses recorded with different calorimeter modules at the CERN test beam facility in fall 2001. The files contain raw data as vectorial sequence of signal voltages as a function of time as it was measured during the tests, including the transmission over a distance of 70 m using prototype cables. The time resolution is $\Delta t_{\mathrm{HEC}} = \Delta t_{\mathrm{TILE}} = 200\,\mathrm{ps}$ for HEC and TileCal and the signal vector length 10 000 points, which corresponds to 2 ms, and $\Delta t_{\mathrm{EM}} = 400\,\mathrm{ps}$ for EM Barrel particles in 2 500 points and 1 ms, respectively.

Software constraints. The signal pulses are mapped to 8-bit values which corresponds to the dynamic range of the graphics card. The time resolution is given by the PIXELCLOCK of the graphics card such that every entry of the 8-bit vectorial vector corresponds to a time interval of 6.25 ns. Furthermore, the specific properties and configurations of the graphics card have to be taken into account, such as the screen resolution, the previously discussed line shift, and moreover that the output of the graphics card is unipolar, whereas the pulse shapes from the LAr calorimeters show the typical undershoot (see section 3.2.1). Being an electrical issue, the latter is not corrected by software, but during the signal conversion on the FAB. However, a virtual baseline must be introduced to be able to simulate the undershoot. This amounts to typically 20% to the signal range, so that the virtual baseline has a level of $\frac{1}{5} \cdot 2^8 = 51$ units.

A software package has been developed using the Qt Development Framework by Trolltech [29], which provides a framework to create a graphical user interface (GUI), methods for image manipulation and functions to write on the screen. It covers the following tasks:

[10] The used driver (appendix A.1) only permits a QUAD-HEAD configuration with a two-fold extended desktop over two screens with a combined resolution of 3200×1200. See 5.1 for details.

[11] No linux driver with 4-HEAD support was available at the time of testing.



scope view
: view of the digital signal, adopted from the screen of an oscilloscope.

view tools
: tools to zoom the signal.

load / save
: load predefined pulse shapes from the pulse library (includes an option to scale)
save to the 8-bit vectorial data format.

standard shapes
: modify the data with some basic functions.

copy / paste
: copy&paste, including the special paste function for multiple insertions and scaling.

log console
: protocols all actions, i.e..copy, paste, etc.

Figure 5.12: The Signal Builder GUI with some typical signals: a clock signal (green), a constant offset signal (blue) and pulse shape of a LAr signal (red).

Creating a pulse sequence. Loading predefined pulse shapes and providing methods to arrange and assemble them in order to match the constraints of the graphics card output with respect to timing and amplitude.

Merging the sequences into a rgb[12]image. Loading the patterns from the previous step and assigning them to a certain colour, while taking into account the fan-out scheme of the subsequent Fan-out and Amplification Board (see section 5.3.1).

Displaying the pattern as picture at full screen. This includes the setup of a very stable and reliable host system for the graphics card, as its output cannot be monitored once the signal chain is completed. The signal chain is shown by figure 5.13.

Figure 5.13: Signal chain of the test setup.

The first two steps are achieved with the *Signal Builder* software. Particular attention was paid to the visualisation of the signal in order to make modifications easy and fail-safe, for which the programme provides a GUI for a direct control over the pulse sequence. Figure 5.12 shows a screenshot of the programme with explanations of the manifold functions.
The data from the pulse library is imported into the *Signal Builder* and scaled to the 8-bit range. The sequence is subsequently assembled by copy & paste actions, while internal routines of the programme take care that the pulses don't exceed the available screen resolution. Apart from the predefined pulses, some basic signal functions like e.g. triangles and sine wave are available.
Pulse sequences are saved in a raw data format that contains a sequence of 8-bit values.

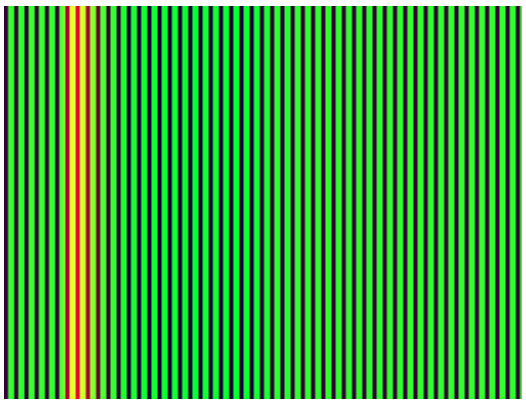


Figure 5.14: Example of an assembled test pattern, consisting of identical lines with a clock signal (green), a constant offset value (blue) and a typical calorimeter pulse with undershoot (red). The image is a screenshot of the signals when displayed on a normal screen.

[12]rgb - red, green, blue.

From the pool of sequences, three are merged into a 24-bit rgb-image (png-format[13]), which is the final format for signal generation. Figure 5.14 shows a part of such an assembled pattern as a screenshot.
The images are displayed by another small application called `displayFS` (A.2) that was written in order to guarantee a reliable full screen readout. At this point it has to be mentioned that any interference from window managers, mouse cursors etc. would result in a perturbing physical signal at the output of the graphics card. It is therefore essential to set up a system that is very stable and reduced to the very basic display functions in order to reduce any disturbing factors a priori. The details of the configuration can be found in A.1.

5.3 Fan-out and Amplification Board (FAB)

A printed circuit board was designed in order to fan out signals from a few channels of the graphics card to a complete 16 channel PPM connector including a transformation of the single-ended signals to differential signals. The required amplitude range is $\pm 2.5\,\mathrm{V}$ for the differential signal and a bandwidth of 20 MHz. This corresponds to the rise time of a typical LAr signal of $\sim 50\,\mathrm{ns}$ and also matches the bandwidth filter that is implemented on the MCM (see section 3.2.2). Furthermore, the results from the preceding chapters concerning gain, baseline shift and the blanking time have to be taken into account.
Because of the complexity of the clock synchronisation, this block was chosen to be realised on a separate device and is described in section 5.4. Hence HSYNC, VSYNC and a channel dedicated to derive the clock signal are routed through the board to be processed externally.

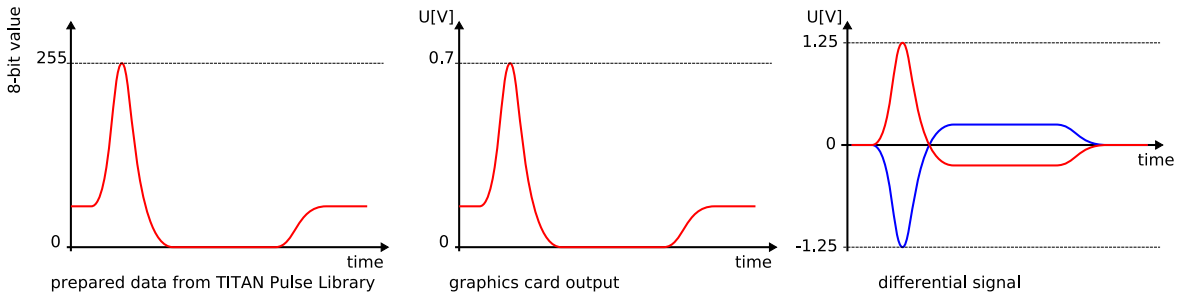


Figure 5.15: Signal processing chain: The template signal pulse data is mapped on the 8-bit output of the graphics card (left), which generates a single-ended unipolar signal (middle). The subsequent step is a shift of the base line, amplification and inverting the signal for the negative branch of the differential signal.

5.3.1 Modularity and Configuration Scenarios

The requirements for the board, apart from the electrical constraints, are a very flexible fan-out scheme in order to be prepared for a variety of different input configurations depending on the availability of synchronous channels as source. In general, a modularity of 16 channels per board was chosen which corresponds to an entire connector to the PPM.

[13] png - Portable Network Graphic. It is a lossless format for 24-bit graphics and includes a prefiltering and the deflate algorithm for a compression of the image data.

The configuration scenarios can be categorised in the following modes:

1-HEAD mode. This is the simplest case when only a single-head graphics card is available, as for example in signal continuity tests in USA15. The source system could be the monitor output of a notebook. However, the output should be available and easily configurable on a subset of up to 16 channels of a PPM connector.
One channel would be used to generate signals, one to produce negative signals by adding its value as offset to the first channel, and another one serves as clock.

External Source. Instead of an input from the graphics card, a standard coaxial lemo input should be provided. The functionality is identical, only the offset feature is not needed then and the clock has to be provided equally from an external source.

4-HEAD mode. Highest possible amount of channels with one graphics card and achieved currently with the Matrox QID Pro. Eight channels are used to produce individual signals, which are duplicated as illustrated in the appendix B.3. Again, two channels are dedicated to the clock and the offset, and two channels are not used.

6-HEAD mode. Assuming that graphics card inter-connection can be achieved and a sufficient amount of channels is available, 6 HEADS can be used to create 16 individual signals plus two channels for clock and offset.

Stack mode. Apart from delivering 16 channels to form a single PPM input connector, the possibility to supply a full PPM is given by the implementation of a inter-board fan-out to duplicate the output using several boards. This should be compatible with all the preceding input modes. Nevertheless, all boards should share identical designs for economical reasons.

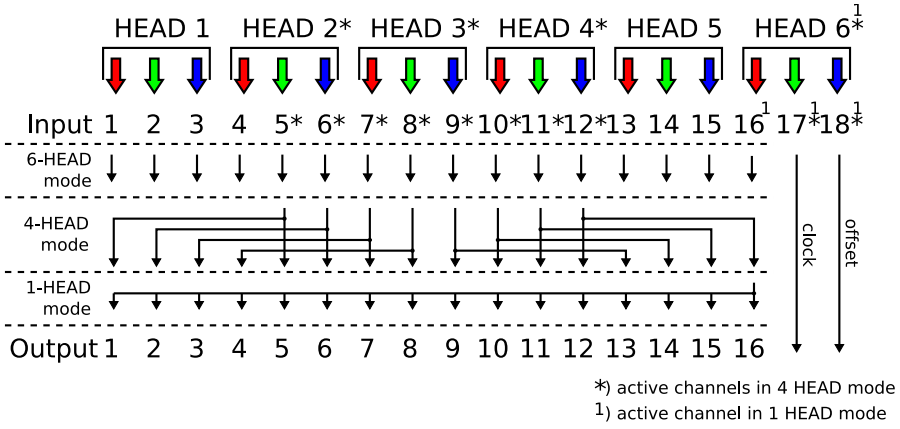


Figure 5.16: Fan-out scheme for the use cases 1 HEAD, 4 HEADs and 6 HEADs.

The fan-out scheme for the different scenarios is shown in figure 5.16. All modes share that the reference clock is deduced from a dedicated channel (CH17, HEAD 6) and that another channel (CH18, HEAD 6) is used to apply a global offset to all channels.

Note: The generation of a L1A[14] was not considered initially, but several possible approaches are discussed in appendix B.3.

[14]L1A - Level-1 Accept TTL signal. See section 3.1.1.

5.3.2 Board Concept

The building blocks of the fan-out and buffer board are:

- **Calibration Stage**, to correct the gain and baseline of the input signals.
- **Offset Stage**, where the inverted signal of CH18 is applied to other channels to shift the baseline.
- **Buffer Stage**, in order to drive the fan-out.
- **Fan-out Stage**, for a flexible distribution of the signals.
- **Differential Output Stage**, which transforms the single-ended into differential signals.

This scheme is applied to all signal channels. Channels 1 to 15 are implemented in the same way, whereas channel 16 also serves as one-for-all source in the 1-HEAD mode.

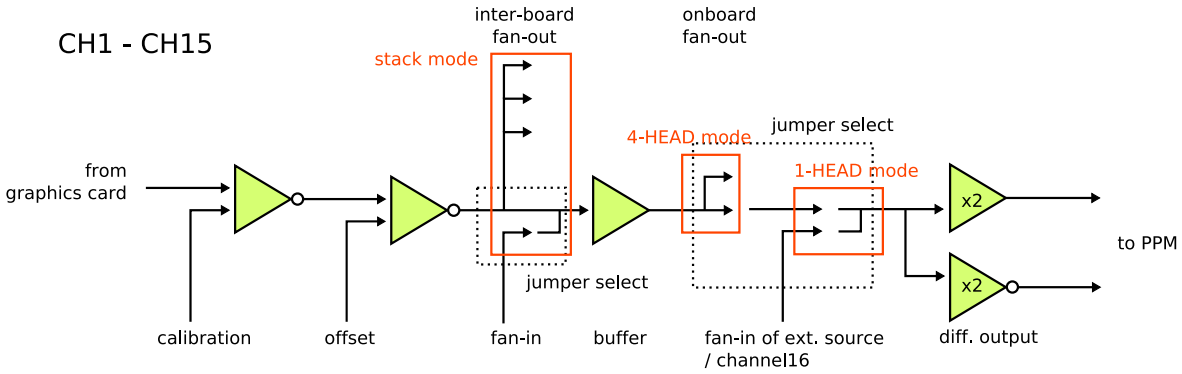


Figure 5.17: Diagram of the signal processing on the FAB of a standard channel.

Standard Channels. Figure 5.17 shows the block diagram scheme of a standard channel, which is the direct result of the building blocks described above. For technical reasons, both the calibration stage and the offset stage invert the signal, which does not change the result, but is important for the baseline shift by the offset channel (see below).
The fan-out scenarios are accommodated at two points. First, the inter-board fan-out (stack mode), which takes place after the signal calibration and baseline shift so that the slave boards receive already corrected signals. The subsequent stages are implemented identically as on the master system. In fact, master and slave boards share the same design.
Second, the fan-out in the 4-HEAD mode is realised in front of the differential output stage. In order to drive the signal for the fan-out, a buffer is introduced beforehand. At the same point, the signal from channel 16 or the external input can be selected as source.

Channel 16. Figure 5.18 shows the building blocks of channel 16. It has, apart from the standard signal path in case of 4- and 6-HEAD mode, an alternative input from an external source and the ability to supply all 16 channels at once (1-HEAD mode), which requires a separate buffer stage with two OPs that provide signals for 8 outputs each.

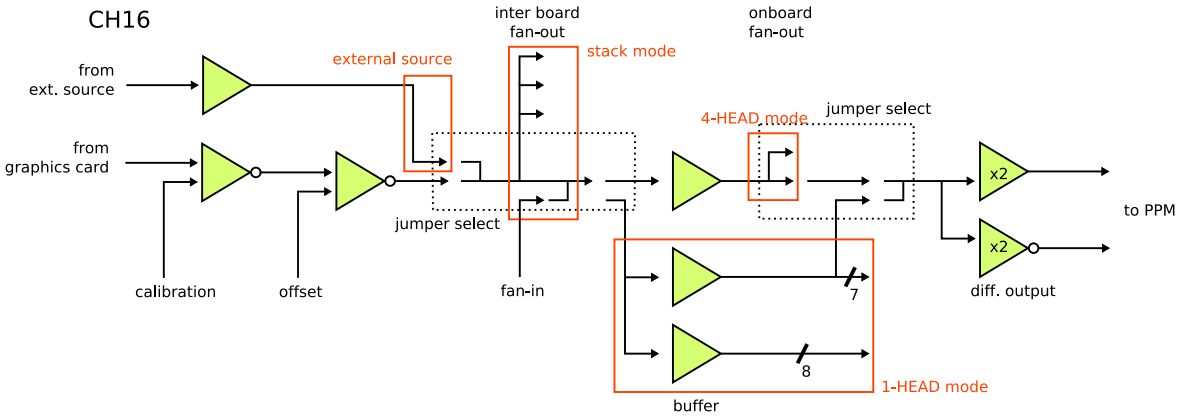


Figure 5.18: Diagram of the signal processing on the FAB of the special channel. It has two possible inputs and an additional buffer stage for the fan-out in 1-HEAD mode where a single input drives all outputs. The red-marked fields indicate the different use cases.

Offset Channel. The offset channel contains a constant voltage level U_{offset} according to the virtual baseline of the pulse sequences introduced in the signal builder software. It is supposed to shift the signal of all channels to the correct baseline, given originally by the template signal pulses from the pulse library. Therefore, the signal of the offset channel is first calibrated to correct for variations in the graphics card output signal and then buffered similarly to the 1-HEAD mode of channel 16 but including another inverting of the signal (see figure 5.19). Thus, adding the offset signal to pulse signals results in a shift of the pulse signal by the (constant) value U_{offset}.
However, during the blanking space, neither the channels 1 to 16 nor the offset channel contain signals, thus the signal voltage is zero at both blanking space and signal period. Nevertheless, timing is an issue as both signals have to compensate each other equally after and before the blanking space. Details of the process are discussed in section 5.3.3.
The timing of the offset stage has to be taken into account in the arrangement of the board as the processing chain of the offset signal not only includes an additional buffer block, but moreover the signal must be distributed equally to all channels throughout the board. To reduce wire length, the offset channel was therefore placed centrally. The block diagram of figure 5.20 shows how the channels are arranged in the final implementation.

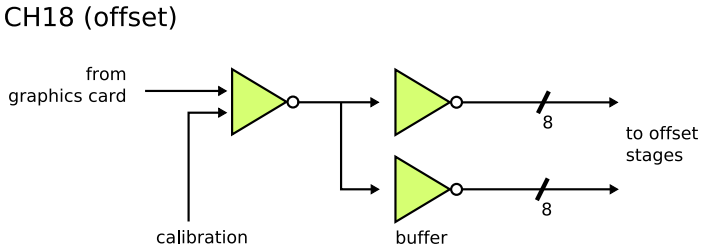


Figure 5.19: Diagram of the offset channel for the signal processing on the FAB. The fan-out is driven by two parallel OPs. Both stages of the offset channel, the calibration and buffer stage, invert the signal.

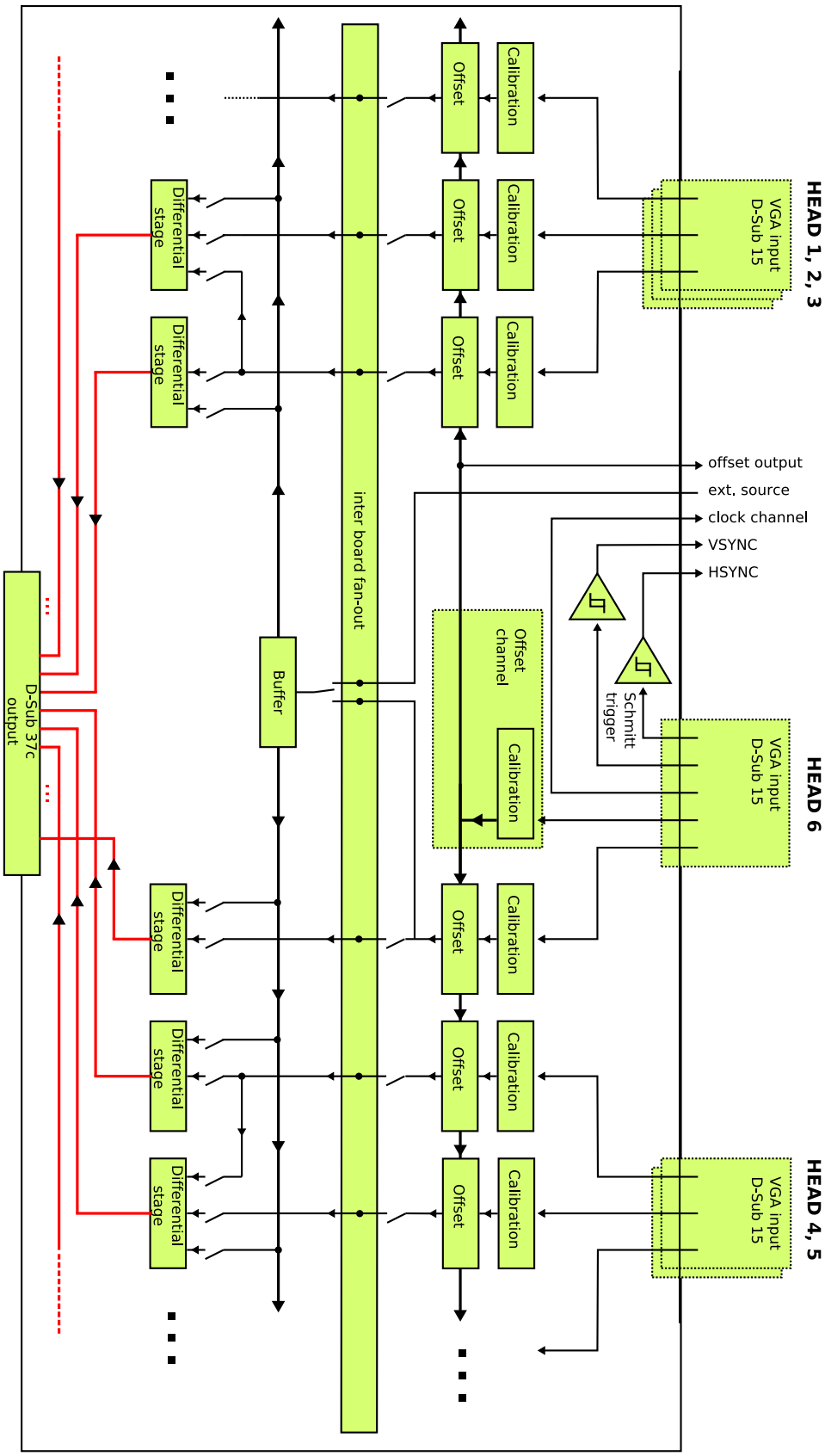


Figure 5.20: Block diagram of the Fan-out and Amplification Board. Black lines indicate single-ended, red lines differential signals. The channels at the left and right hand side are not fully drawn.

Symbol	Parameter	Unit	LT1813	OPA650	OPA820[17]
−3 dB BW	−3 dB bandwidth	MHz	see fig. 5.32	see fig. 5.33	see [31]
GBW	Gain Bandwidth Product	MHz	100	180	280
I_{in}	Input Bias Current	μA	4	20	16
I_{out}	Output Current	mA	40	> 65	> 75

Table 5.2: Characteristics of the operational amplifiers (excerpt from [32], [33], [31])

5.3.3 Implementation and Measurement

The underlying electronical implementation makes manifold use of operational amplifiers. Therefore, their basic functionality will be discussed in the following.

Introduction to Operational Amplifiers Circuits

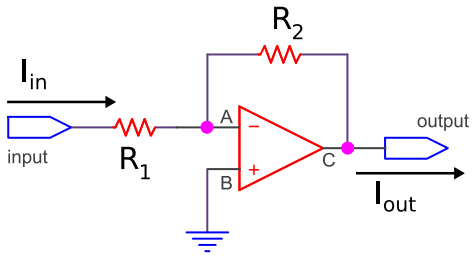
The behaviour of operational amplifiers with negative external feedback in an electronic circuit can be fully[15] explained by two *Golden Rules* [30]:

Rule 1 The output of the operational amplifier always tries to even out differences at its input levels.

Rule 2 The inputs (almost) draw no current. Typical values of the used OPs are shown in table 5.2.

Rule 1 also leads to the *concept of virtual ground*: if one of the inputs is connected to ground, the operational amplifier attempts to set the other input to ground too, which is then called virtual ground. This is very helpful to understand and to design circuits using operational amplifiers.

OPs as inverting amplifier



Rule 1 implies that both inputs are at the same voltage, hence they are both at GND[16]. Rule 2 says that no current is drawn from the input, thus using Kirchhoff's Circuit Laws the currents at point A can be written as

$$I_{\text{in}} + I_{\text{out}} = \frac{U_{\text{in}}}{R_1} + \frac{U_{\text{out}}}{R_2} = 0.$$

Thus

$$\text{voltage gain} = \frac{U_{\text{out}}}{U_{\text{in}}} = -\frac{R_2}{R_1}.$$

The minus sign indicates that the output voltage is inverted.

[15] Exception: inputs and outputs must not be saturated at one of the supply voltages; the OP has to be in the active region.

[16] GND - ground.

[17] The TI OPA820 is the recommended upgrade package for the outdated TI OPA650.

OPs as non-inverting amplifier

The non-inverting amplifier is very similar to the inverting amplifier. Again, Rule 1 states

$$U_{\text{in}} = U_{\text{B}} \stackrel{!}{=} U_{\text{A}}.$$

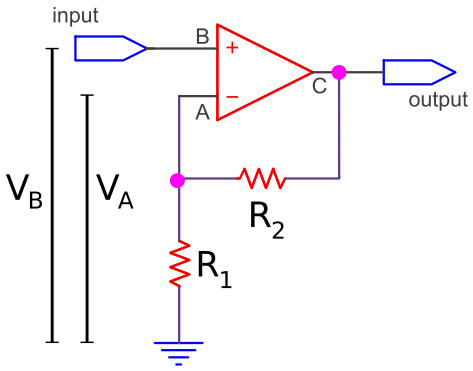
The resistors R_1 and R_2 form a voltage divider with

$$U_{\text{A}} = U_{\text{out}} \frac{R_1}{R_1 + R_2},$$

hence

$$\text{voltage gain} = \frac{U_{\text{out}}}{U_{\text{in}}} = 1 + \frac{R_2}{R_1}.$$

The minimum gain of a non-inverting amplifier is thus 1.



Another important property of OPs, being active elements, is that they buffer incoming signals. As stated by Rule 2, they only draw very few current, thus ideally have infinite impedance and don't load the input signal. On the other hand, the output is *active*, meaning that they can bear higher output currents than the signal at the input. However, the behaviour of OPs is optimised to drive low resistive and capacitive loads and therefore, a four fold fan-out of the signal after every buffer was considered as a moderate number in order to achieve a good high-frequency behaviour.

The basic electronic building blocks of the FAB are the operational amplifiers OPA650 from Texas Instruments [33] and LT1813 from Linear Technology [32]. The packages have been chosen for their compactness and good bandwidth characteristics (see table 5.2). They serve as buffers for the incoming signals and drivers for the fan-out as well as amplification blocks.

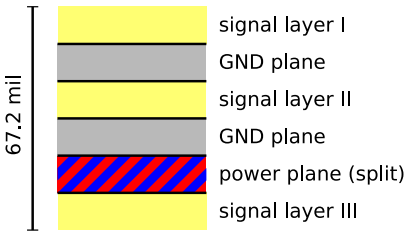


Figure 5.21: Profile of the printed circuit board (not drawn to scale). The layer stack up is symmetrical, with a thickness of 1.37 mil[18] for the signal routing layers, separated by 11.8 mil cores. The signal layers are shielded through GND layers. The power supply ($U_{\text{E}} = +5\,\text{V}$, $U_{\text{CC}} = -5\,\text{V}$) is realised as split plane.

Fan-out and Amplification Board

For the circuit design and layout, the *Cadence Allegro package* [34] was used. The guideline on the layout were compactness of the individual channels in order to minimise crosstalk between channels, and reducing wire length in general to a minimum, which includes the central positioning of the offset channel. Furthermore, the possibility to implement a bandwidth

[18] mil - milli-inch. 1 mil = 25.4 µm.

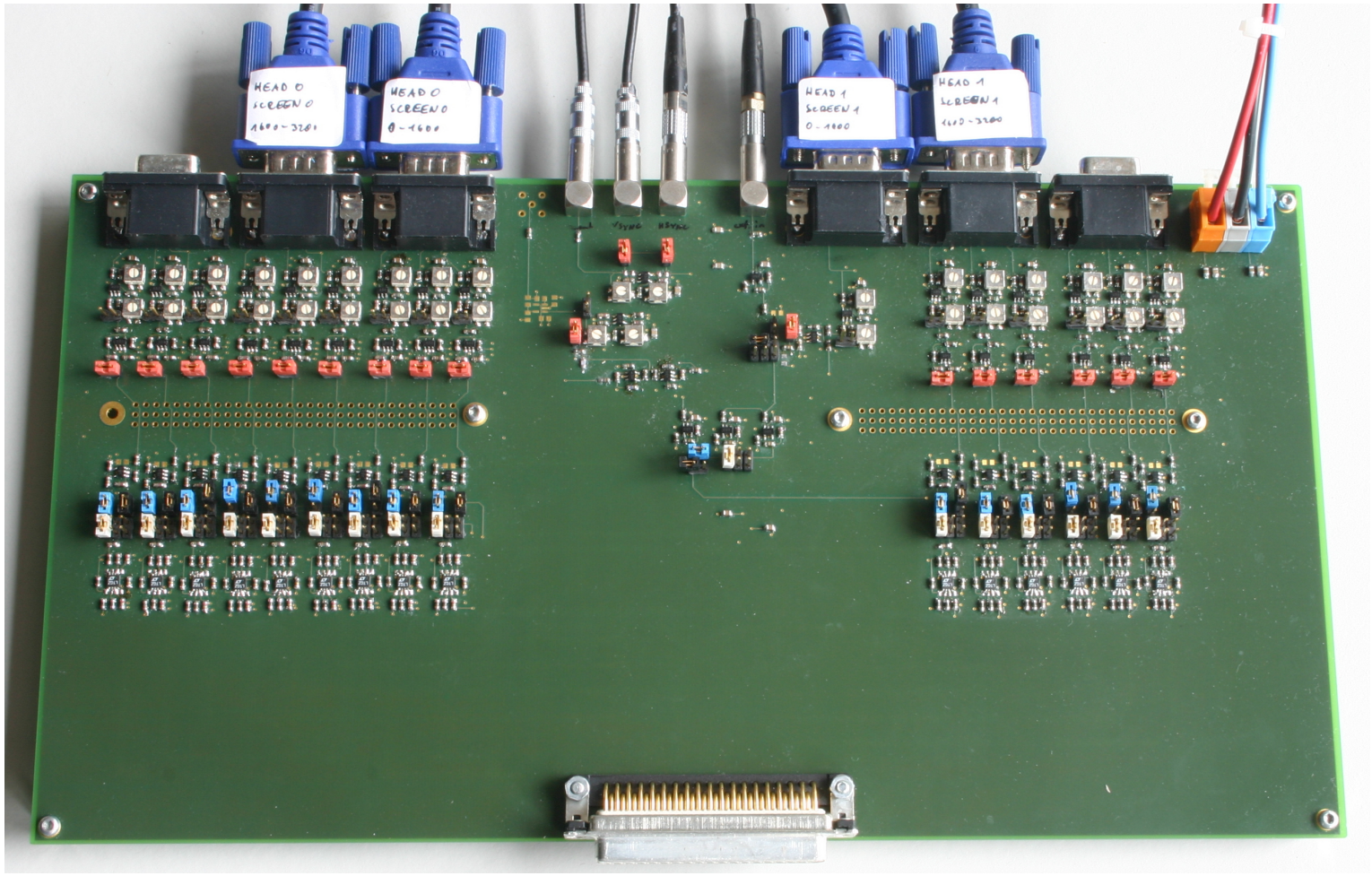


Figure 5.22: Photograph of the Fan-out and Amplification Board (FAB). The board is set up for the 4-HEAD mode, and four graphics card's connectors are plugged in at the input. Each channel has two potentiometers to adjust gain and offset. The jumpers colour code is as follows: *red* connects/disconnects the input stages if the stack mode is used, *blue* and *black* handle the fan-out and *white* selects between 4-HEAD (and also 6-HEAD) mode and 1-HEAD mode (see figure B.2 in appendix B.1).
The two inter-board fan-out connectors of type VG96 are not assembled at this point as well as a buffer stage to make the offset channel externally available.

filter to reduce high frequency noise was foreseen for every channel. The resulting printed circuit board (PCB) is a six-layer board, consisting of a split power plane and three signal routing layers that are shielded by two ground planes as illustrated in figure 5.21. The total size is 316 mm × 169 mm, thus non-standard dimensions. The board was manufactured by Würth Elektronik [35]. Figure 5.22 shows a photograph of the board.

Calibration Stage

The outputs of the graphics card are very precise concerning linearity. However, they differ in offset and maximum values. Therefore, the signals have to be normalised in respect of baseline voltage and gain.

Figure 5.23 shows the implementation of the calibration stage. It consists of an inverting

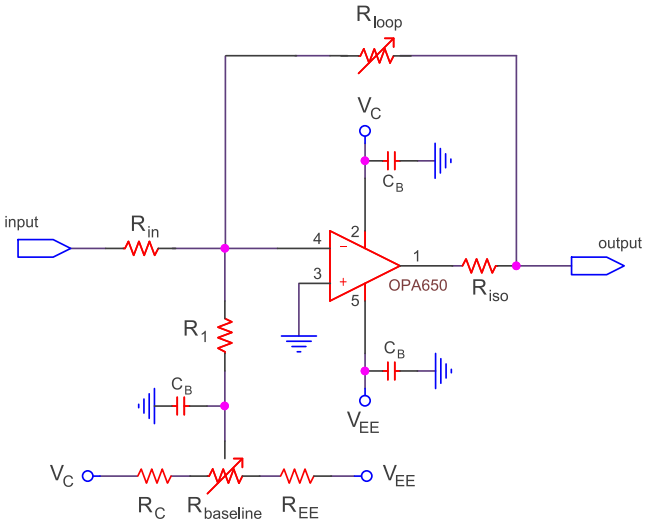


Figure 5.23: Schematic of the calibration stage. The potentiometers allow an adjustment of gain and voltage baseline.

operational amplifier with variable gain and a loaded voltage divider. A potentiometer is implemented as loop resistor R_{loop} with values in between 500 Ω and 1.5 kΩ to allow for a gain in the range of 0.5 to 1.5 (with $R_{\text{in}} = 1\,\text{k}\Omega$). This is satisfactory to calibrate the maximum input voltage. R_{iso} is 22 Ω and therefore negligible.

The calibration of the baseline is achieved via a loaded voltage divider, which adds a voltage to the signal by Kirchhoff's Voltage Law at pin 4 of the OP. In order not to draw too much current from the input, a high value of 10 kΩ is chosen for the voltage divider resistors R_1, R_{C}, R_{baseline} and R_{EE}.

The OP's output is sensitive to capacitive loads since they cause oscillations. Hence, the resistor $R_{\text{iso}} = 22\,\Omega$ is added to isolate the parasitic capacitive loads of the subsequent conductor paths [33]. Furthermore, the several block capacitors $C_{\text{B}} = 100\,\text{nF}$ limit the high frequency noise of the circuit. The following oscilloscope pictures show channel 16 containing a sequence of predefined pulses from the TITAN pulse library. It is a repetitive pulse from a 120 GeV electron, measured in a test setup with a module of the electromagnetic barrel, including the 70 m of cables before the PreProcessor. The resulting amplitude is $U_{\text{max}} = 0.656\,\text{V}$, which was taken for testing purposes without any corrections for e.g. cable attenuation. Figure 5.24

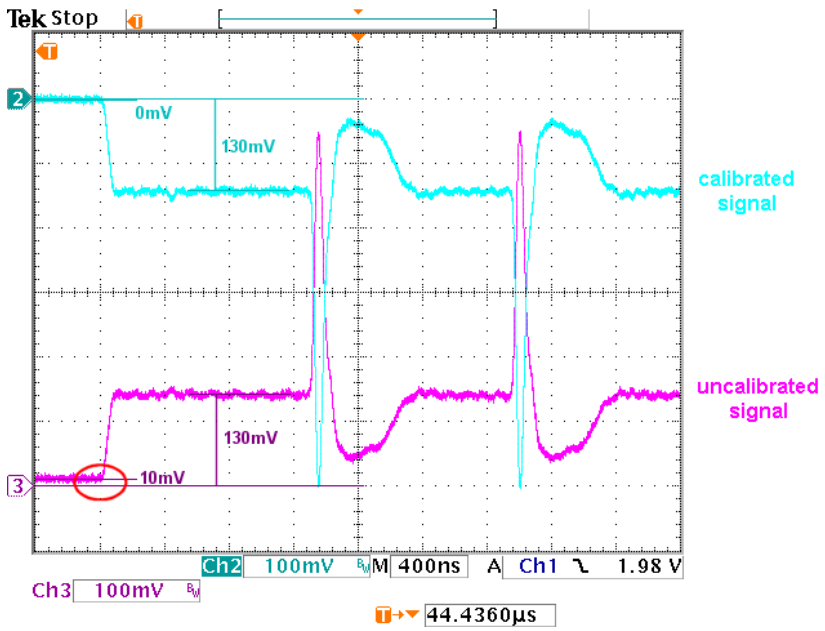


Figure 5.24: Signal before (CH3, pink) and after the calibration stage (CH2, cyan). The signal consists of a pulse sequence with a virtual baseline of $\sim 130\,\mathrm{mV}$. During the blanking space (very left on the scope screen), the baseline voltage of the uncalibrated signal differs from zero by $\sim 10\,\mathrm{mV}$, which is corrected by the calibration stage. Additionally, it is inverted for technical reasons and the gain is adapted such that the voltage of the peak equals 800 mV.

shows the beginning pulse sequence at the input of the board and after the calibration stage.

Offset Stage

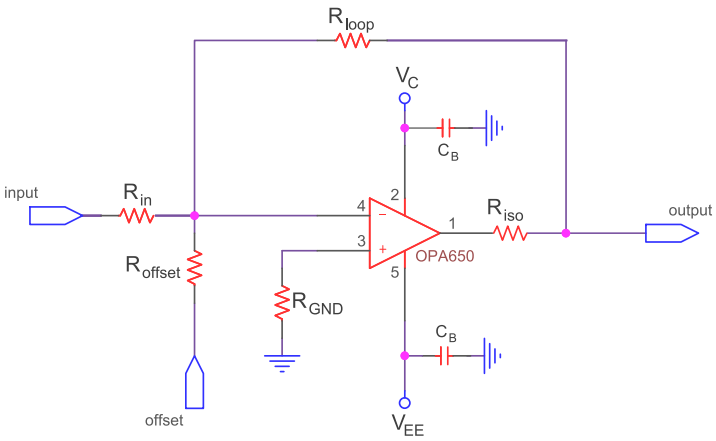


Figure 5.25: Schematic of the offset stage for a standard channel. Both signal and offset are merged at the inverting input, which is virtual ground.

With the offset stage, the baseline can be shifted in order to achieve negative signals, although the graphics card only produces positive signals. As described in section 5.3.2, the

inverted signal of the offset channels is added to all other signal channels (CH1-CH16), which shifts the voltage baseline of all signals by the (constant) value of CH18. The schematic of the offset stage (figure 5.25) is very similar to the calibration stage. The main building block again is an OP in an inverting circuit with positive input connected to ground, allowing for the addition of the voltage U_{offset} at pin 4. The gain is 1 since

$$\text{gain} = \frac{R_{\text{loop}}}{R_{\text{in}}} = \frac{R_{\text{loop}}}{R_{\text{offset}}} = \frac{1\,\text{k}\Omega}{1\,\text{k}\Omega}.$$

The offset application is sensitive to the right timing in relation to the signal channels at the

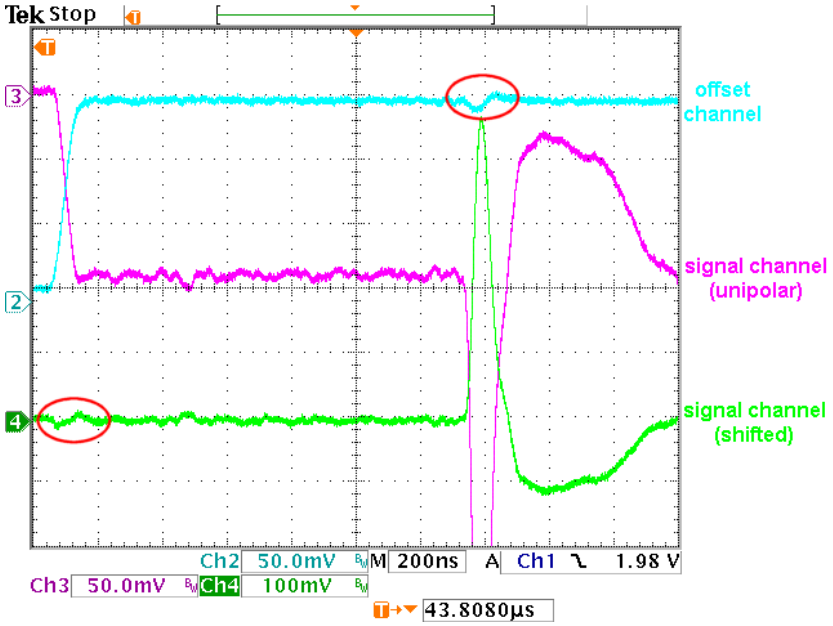


Figure 5.26: Offset stage. Signals from offset signal (CH2, cyan) and the pulse sequence on channel 16 (CH3, pink) are merged, resulting in the signal on CH4 (green) with a distortion of 20 mV (red circle on left hand side). Another effect that can be seen on the picture is crosstalk from CH16 to the offset channel at the peak of the pulse sequence (red circle on the right).

beginning and the end of the blanking space since both signals have to reach the virtual offset voltage level at the same time. As the offset includes an additional buffer stage and routing, which results in a delay of approximately 15ns in comparison with the signal from the channels 1 to 16, a correction by software was introduced: First a compensation by a 3 px $\rightarrow$ 18.75 ns shift of the offset channel compared to channel 1 to 16, and second introducing a slope such that both signals reach the virtual baseline not at once but after 10 px and successively cancel out each other. The result of the process is shown in figure 5.26. Though not perfect, the effect could be reduced to distortions with a maximum amplitude of 20 mV.

Differential Output Stage

The differential output stage provides the non-inverted and the inverted branch of the differential signal. Both branches are amplified with a gain of 2 ($R_{\text{in-}} = 1\,\text{k}\Omega$, $R_{\text{loop-}} = 2\,\text{k}\Omega$

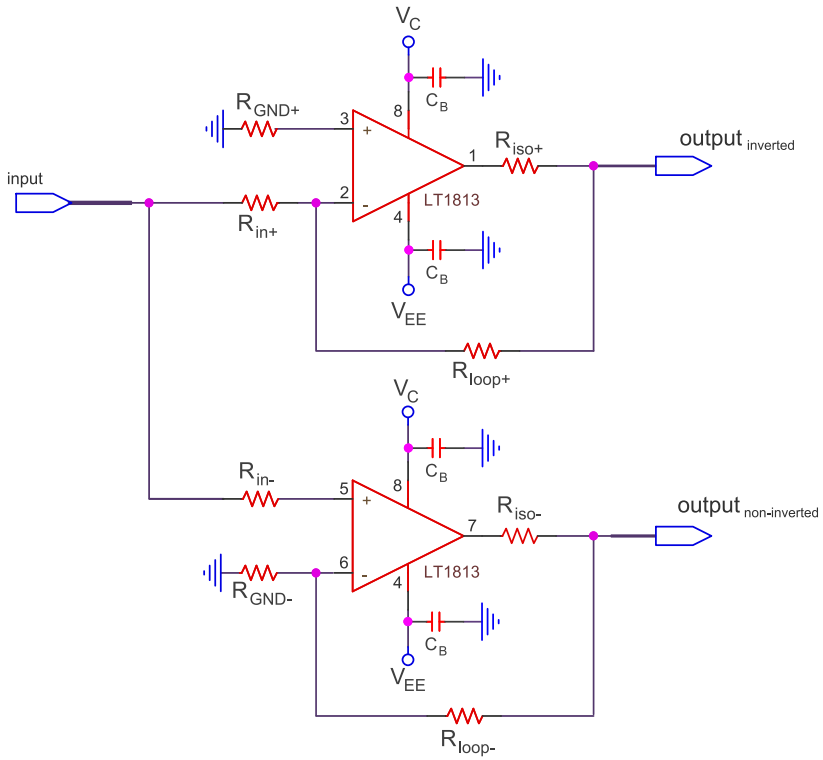


Figure 5.27: Schematic of the differential output. It consists of two OPs in inverting and non-inverting circuit, both with gain 2, for the two branches which form the differential signal. Each then has an amplitude of $U_{\max} = 1.25\,\mathrm{V}$ and hence $|V_{\mathrm{diff,\,max}}| = 2.5\,\mathrm{V}$.

and $R_{\mathrm{in+}} = 1\,\mathrm{k\Omega}$, $R_{\mathrm{loop+}} = 1\,\mathrm{k\Omega}$), thus the total gain is 4, not including the maximum amplification of the calibration stage by another factor of 1.5.

In contrast to the other building blocks, the LT1813 package was chosen as OP due to its compactness and the fact that it is available in a dual package with two OPs combined in one chip, which is favourable concerning equal rise times. Figure 5.27 shows the two branches of the differential signal and the final output.

5.3.4 Board Performance

Linearity

The linearity was determined at both the board input which corresponds to the graphics card output and at the boards differential output in a combined measurement. The method is identical with the measurement of the graphics card output characteristics (see section 5.1). Figure 5.29 shows the linearity as the difference of measured and fitted values vs. the original digital data. The linearity of the FAB output (red) differs within less than 1% and deviations are basically inherited from the graphics card (blue).

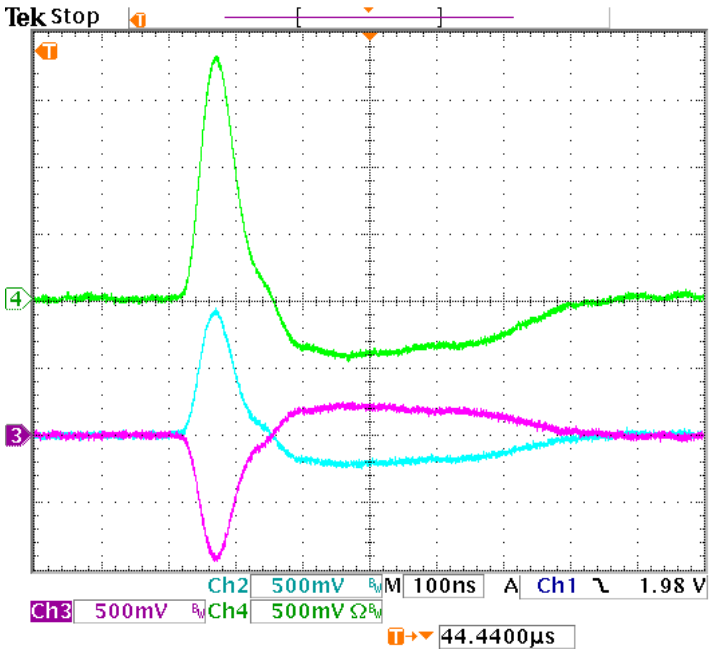


Figure 5.28: Signal at the output stage. CH2 and CH3 are the two branches of the differential signal. CH4 shows the final output, measured with a differential probe. A bandwidth filter of 20 MHz corresponding to the MCM's input filter is applied on all channels.

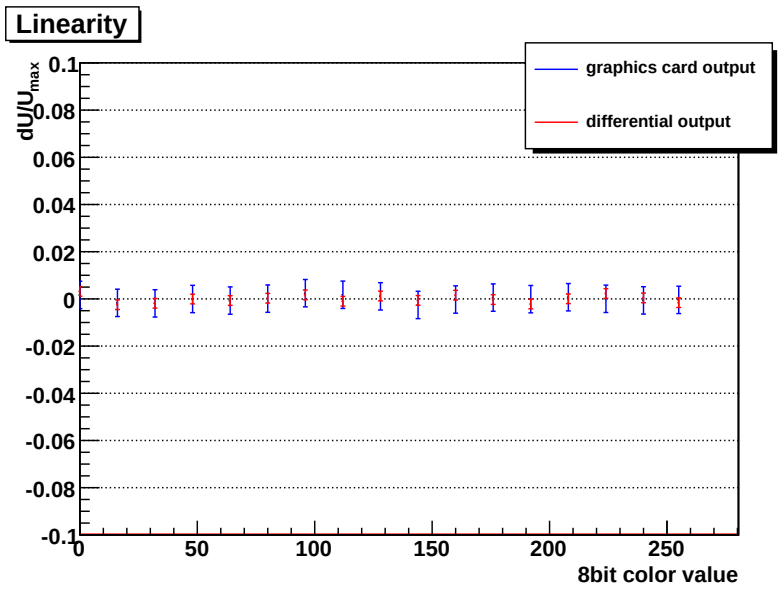


Figure 5.29: Linearity of the FAB as difference of measured and fitted values vs. digital data. Additionally, the linearity of the graphics card is shown.

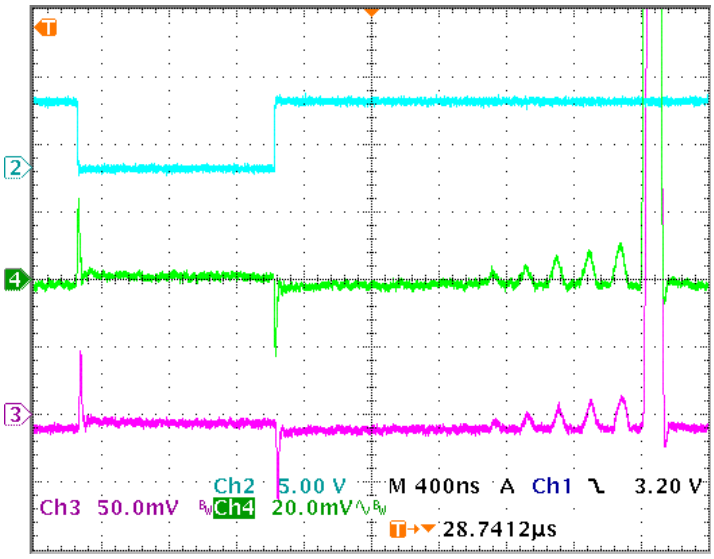


Figure 5.30: Noise and crosstalk. CH2: HSYNC, CH3: board input, CH4: differential output. A 20MHz filter is applied.

Noise and Crosstalk

The noise was analysed for the signal chain as a whole. This includes primarily the low-pass filter which is implemented on the MCM in front of the FADC and eliminates high frequency noise. Hence, the noise estimation only takes into account noise below a frequency of 20 MHz. Furthermore, it should be noted that the measurement of electrical noise is dominated by noise from the tectronix probes and the oscilloscope. Therefore an upper limit of $\mathrm{RMS}_{\mathrm{noise}} \leq 5\,\mathrm{mV} \hat{=} 1\%$ was determined, which is negligible considering the amplitude of the calorimeter pulse and the intrinsic noise of the calorimeter signal.
Thus, the dominating noise factors rather originate from the graphics card as stated in section 5.1, namely crosstalk from the HSYNC and VSYNC signals. How crosstalk and electric noise relate is shown in figure 5.30. On the right hand side, five peaks stick out of the base line with rise times of 50 ns and increasing amplitudes from $A_1 = 2.73\,\mathrm{mV}$ to $A_5 = 5 \cdot A_1 = 13.6\,\mathrm{mV}$. The peak with an amplitude of 1 almost vanishes within the noise, but comparison between the signal at the input (CH4, green) and the signal at the output (CH3, pink) also shows that the main source for noise is the measurement itself as the noise level is basically constant although the amplitudes differ with a factor of 2. The left hand side points out the influence of the HSYNC signal during the blanking space. The resulting spikes have an amplitude of $\sim 25\,\mathrm{mV}$, which corresponds to 11 units in terms of the graphics card colour brightness. This is unavoidable and must be considered as the minimum noise. However, the appearance of the crosstalk from the synchronisation pulses is predictable and can eventually be taken into account.
Nevertheless, also crosstalk between channels of the same HEAD is noticeable. A problem emerges primarily from the clock channel on HEAD6, as it has a fast rise time of 6.25 ns and a high amplitude. This affects not only channel 16 but foremost the offset channel and thus all other channels. To limit the effect, the possibility to place a 20 MHz low-pass was used in this case. This effectively reduces crosstalk, but with the offset signal being smoothed out a bit, the offset application process, as described in section 5.3.3, suffers as the two signals

noise source	order
electric noise	5mV (localised)
crosstalk from HSYNC, VSYNC	25mV (localised)
crosstalk from clock channel	25mV (localised)
offset application process	20mV (localised)
crosstalk from signals	15mV (localised)

Table 5.3: Main noise sources. Almost all of them can be traced back to the graphics card. Values are taken before the amplification by a factor of 4 at differential output stage, with 20MHz filter applied.

do not cancel out completely anymore. Thus, the inherited noise from the clock channel causes a distortion of the signal in the order of 20 mV during the offset application process. Furthermore, crosstalk up to 15 mV from regular channels with typical calorimeter pulses is also observed (figure 5.26).

The noise effects are summarised in table 5.3. Concluding, the main source of noise is the graphics card, with a maximum distortion of ~ 25 mV. However, the origins are well known and the appearance can be predicted very precisely.

Frequency Characteristics

Figure 5.31 shows the frequency characteristics of the FAB. It was measured at the positive output of the differential signal using a sine wave with $U = 600$ mA from a signal generator

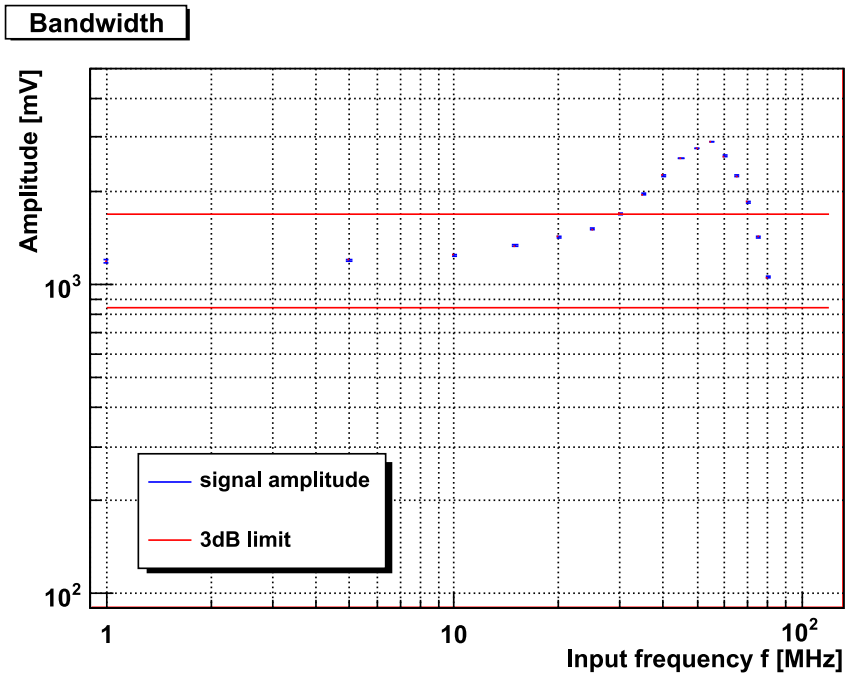


Figure 5.31: Frequency response of the VCO board at the positive signal of the differential output. Input was a sine wave with $U = 600$ mA.

connected to the input channel *external source*.

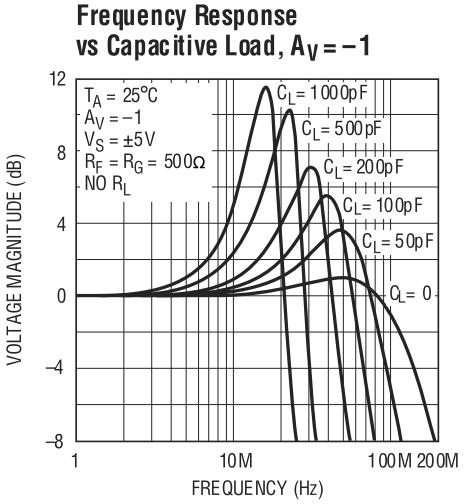


Figure 5.32: Frequency response of the LT1813. The OP is very sensitive to capacitive loads at the output [32].

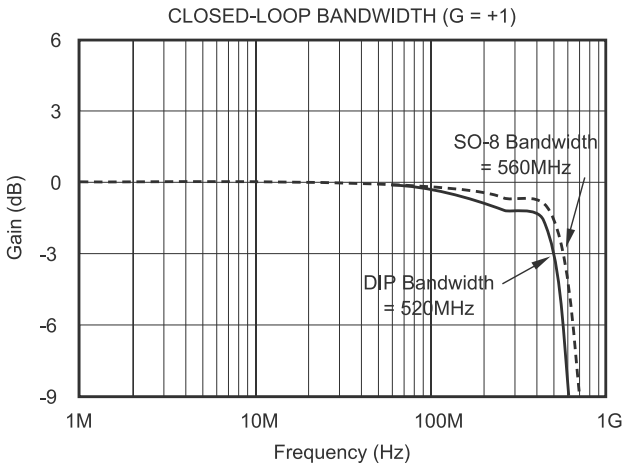


Figure 5.33: Frequency response of the OPA650 [33].

As bandwidth limit, i.e. the frequency when the signal amplitude of the output voltage U_{output} exceeds the 3dB bandwidth limit was examined. The frequency response shows an extensive overshoot for frequencies above 30 MHz. This is due to the sensitivity of OPs to capacitive loads at the output, as shown exemplarily by figure 5.32, which is the frequency response of the LT1813 for various output capacitances. In order to minimise the undershoot, an additional low-pass filter would be necessary by introducing another resistor at the output of the amplifier circuit. This should be part of further investigation to optimise the board's performance. Nevertheless, the achieved bandwidth is in very good compliance with the requirement of simulating pulses with a rise time of 50 ns $\hat{=}$ 20 MHz.

5.4 Clock Synchronisation

To achieve a synchronous timing of analogue signals and the 40 MHz clock, one channel from the graphics card is used as a reference clock. This has the advantage of a very stable phase between clock and signals within the signal period as both are deduced from the same PIXELCLOCK on the graphics card.
The challenge in this approach is to bridge the blanking time gap of the graphics card output since the system clock has to be provided continuously for the operation of the PPMs. Therefore a *Phase-Locked Loop* (PLL) with a *voltage controlled oscillator* (VCO) was set up to create a 40 MHz clock using the graphics card clock signal as a reference instead of the clock itself. With this approach, the clock signal during the blanking time can be obtained by holding the control input of the VCO at the last known value before the gap.

5.4.1 Level Converter

As described in section 5.1 the graphics card output amplitude lies within a range of 0 V and 0.7 V. To make this analogue signal suitable for the digital input of a TTL logic[19], it has to be transformed in order to fit the low- and high-level input voltages of the given device. Thus a gain of factor 4 and a base line shift has to be achieved.
A single stage common base level converter consisting of a NPN-transistor in grounded-base circuit as shown in figure 5.34 is a fast and easy implementation.

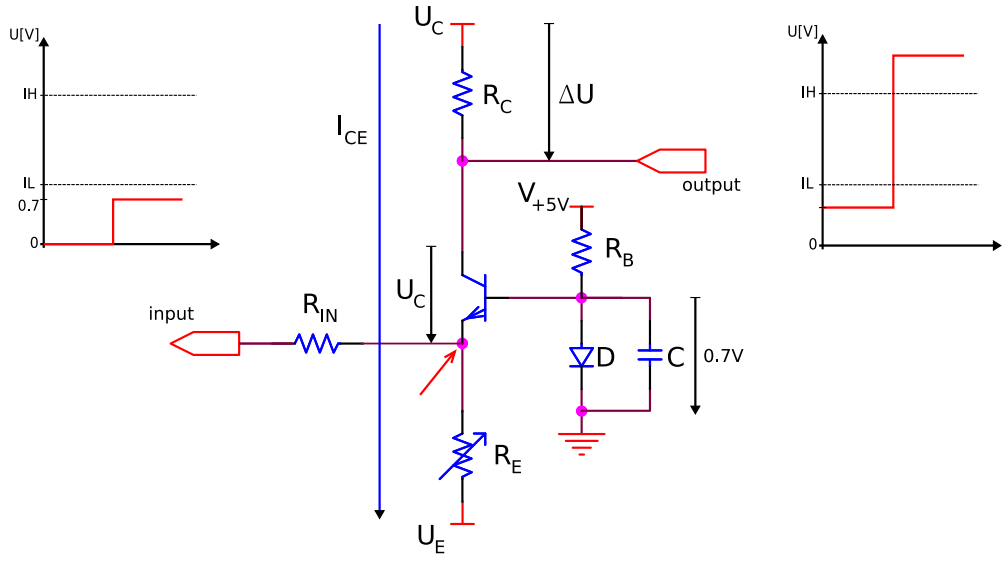


Figure 5.34: Schematic of a level converter with input (left) and output voltage (right) for the low and the high state. The red arrow indicates the point of virtual ground.

To understand the circuit, we refer to the concept of virtual ground. The diode and the block capacitor assure a very stable working point for the transistor base since it causes a

[19] TTL - Transistor-transistor logic; A TTL signal is defined as *low* when U_{IN} is in between 0 V and $U_{IL} = 0.8$ V and *high* between $U_{IH} = 2.0$ V and 5.0 V.

voltage drop of 0.7 V to GND which corresponds exactly to the voltage drop of the base-emitter junction in the NPN-transistor. The emitter is at virtual ground, and a constant current I_{CE} flows.
Supposing that the input voltage is zero and there is no input current at R_{IN}. Then, I_{CE} is regulated by the resistor R_E by Ohm's Law since $I_{CE} = I_E = \frac{0\,V - U_E}{R_E}$. The same current I_{CE} is passing R_C, which results in a voltage drop of

$$\Delta U_L = R_C I_{CE} = \frac{R_C}{R_B}|U_E|.$$

This defines the low-level and the resulting voltage at the output is $U_L = U_C - \Delta U_L$.
With a signal at the input, an additional current $I_{IN} = \frac{U_{IN}}{R_{IN}}$ is fed in at the emitter reducing the current between emitter and collector such that

$$\Delta U_H = R_C\,(I_{CE} - I_{IN}) = R_C \left(\frac{|U_E|}{R_E} - \frac{U_{IN}}{R_{IN}}\right).$$

Thus the gain is

$$gain = \Delta U_H - \Delta U_L = R_C \left(\frac{|U_E|}{R_E} - \frac{U_{IN}}{R_{IN}}\right) - \frac{R_C}{R_E}|U_E| = R_C \frac{U_{IN}}{R_{IN}}$$

and depends only on R_C. If that value is fixed, the variable resistor R_E defines the offset and can be used to shift the signal such that it fits symmetrically the high- and low-levels of the TTL (see section 5.35).

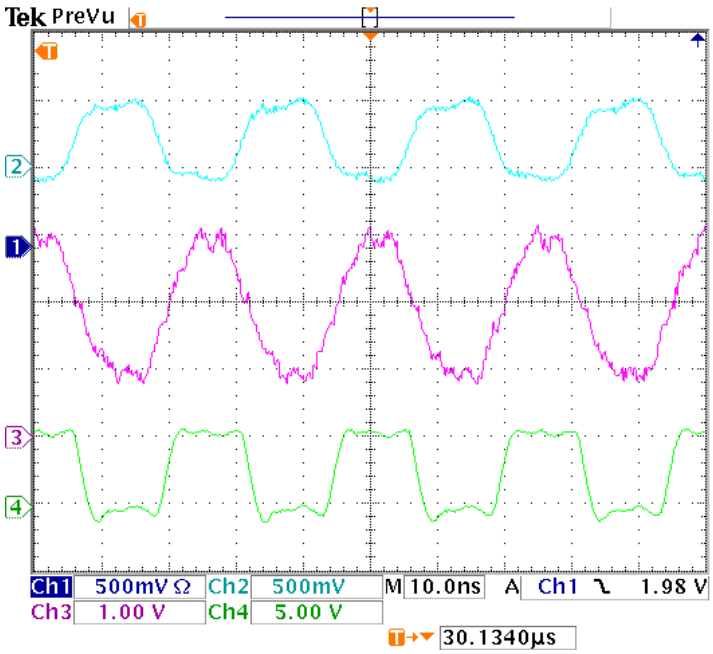


Figure 5.35: Clock signal at the input of the level converter (CH2, cyan), at the output (CH3, pink) and after passing a CPLD (CH4, green).

R_{IN} serves as terminating resistor for the video signal cable and is fixed at $R_{\mathrm{IN}} = 75\,\Omega$. From $gain = 4$ follows $R_{\mathrm{C}} = 300\,\Omega$ and $R_{\mathrm{E}} \approx 300\,\Omega$ ($R_{\mathrm{E,\ measured}} = 293\,\Omega$). For C_1 a common value of 100 nF was chosen and $R_{\mathrm{B}} = 1\,\mathrm{k}\Omega$.

The resulting signal is shown in figure 5.35. The signal baseline could be shifted such that the clock signal at the output of a TTL device is highly symmetric (see section 5.4.3).

5.4.2 Concept of Phase-Locked Loop

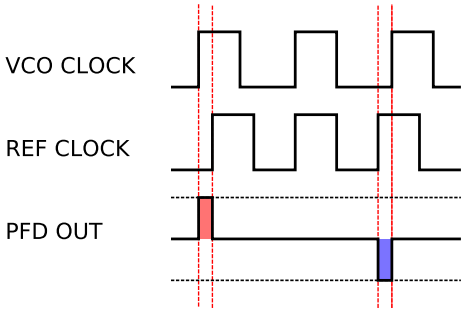


Figure 5.36: Phase frequency detector (PFD) timing chart. The PFD compares the phases of the voltage controlled oscillator and the reference clock. In case that they differ, it generates a positive output voltage U_{IH} resp. a negative voltage U_{IL}, otherwise maintains a high impedance state *Hi-Z* [36].

A phase-locked loop (PLL) is a mixed analogue / digital circuit that generates a clock signal synchronous to a reference clock. The building blocks of such a PLL are: a *voltage controlled oscillator (VCO)* with a bias frequency $f_{\mathrm{VCO,\ bias}}$ close to the reference clock f_{ref}; a phase detector, also referred to as *phase frequency detector (PFD)*, which compares two input frequencies f_{ref} and f_{VCO} and generates an output voltage corresponding to their phase difference. It is in high-impedance state (Hi-Z, see figure 5.36) if the phase difference is within the limit ($< 1\,\mathrm{ns}$); a *loop filter* which is supposed to smooth abrupt changes from the PFD output to guarantee stable running conditions. In the simplest case, this is a low pass filter with a capacitor which maintains the voltage for the VCO input when the PFD output is in Hi-Z ; a *frequency scaler* (divide-by-N counter) to create multiples of the reference frequency. The principle is illustrated in figure 5.37.

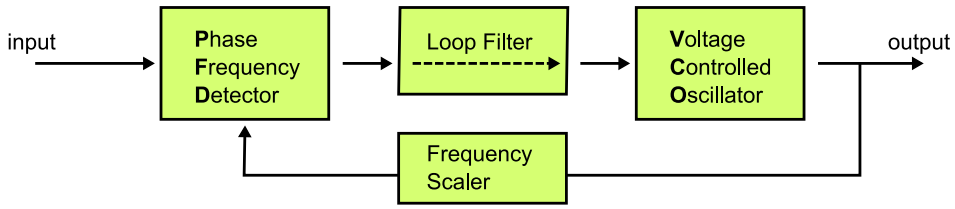


Figure 5.37: Phase-Locked Loop

The package that was used for realisation is a CMOS technology based chip [36] that combines both a VCO and an edge-triggered type PFD, either with an *INHIBIT* function to set the output voltage level to low respective high-impedance state. This feature allows the VCO to run freely in the blanking time gap when the PFD output is inhibited and the VCO input voltage is maintained only by the loop filter capacitor (see section 5.4.5).

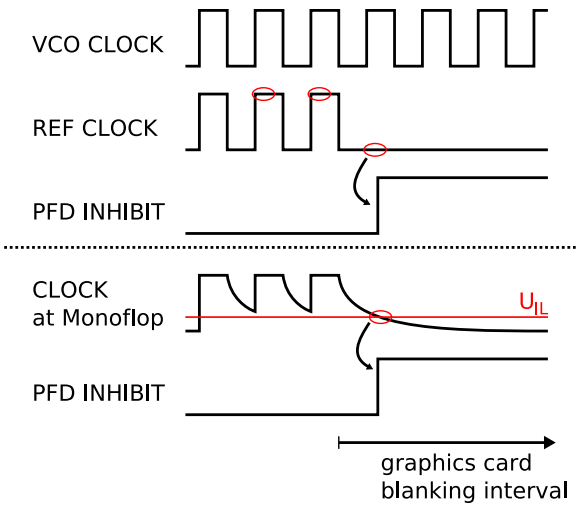


Figure 5.38: Illustration of the PFD INHIBIT function. When the reference clock stops, the PFD output must be placed in the high-impedance state at once.

5.4.3 CPLD routing

All inputs and outputs of the system except for the loop filter are connected through a CPLD[20]. This makes it possible to keep the system configurable and to derive information for other purposes as the mentioned PFD INHIBIT (see section 5.4.4).
A CPLD consists of multiple logic blocks, called *Macrocells*. These can be freely connected between themselves and to the I/O pins through a routing matrix. The configuration is programmed via a JTAG interface[21] and the memory is non-versatile.
Furthermore, the use of the CPLD has the advantage that it is capable of driving a $50\,\Omega$ coaxial cable if two output pins are combined since the required current for a signal amplitude of $U_{\mathrm{OH}} = 2.4\,\mathrm{V}$ is

$$I_{\mathrm{req}} = \frac{U_{\mathrm{OH}}}{50\,\Omega} = 48\,\mathrm{mA}$$

and $I_{\mathrm{OH}} = 24\,\mathrm{mA}$ [37]. This relieves the VCO output as it would disturb the oscillation if it had to carry big loads.
The circuit was designed for a supply voltage of $U_{\mathrm{CC}} = 5\,\mathrm{V}$.

5.4.4 Blanking Space and Monoflop

Assuming that the Phase-Lock Loop is implemented in an efficient way (see section 5.4.5), the focus is on triggering the PFD INHIBIT immediately when the blanking space starts. This information should be derived from the reference clock, as illustrated in figure 5.38, by the CPLD. It then occurs that the first non-existing pulse can only be measured with an additional timing interval. To avoid complications while the VCO and the reference clock are not synchronised yet, a different approach was chosen by introducing a monoflop as a separate building block. The monoflop is realised by a capacitor that is loaded via a diode D and a resistor R in parallel (see figure 5.39). The input is connected to the reference clock via the CPLD. When the input is in high state, the capacitor is charged. The diode guarantees a fast charging time, whereas the resistor R limits the discharge when the input state is low. The value for R is chosen such that the voltage drop below U_{IL} is achieved in only little more than

[20] CPLD - Complex Programmable Logic Device.
[21] JTAG - Joint Test Action Group, IEEE 1149.1.

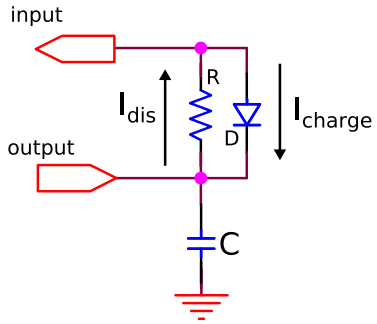


Figure 5.39: Schematic of a monoflop, also often referred to as *monostable multivibrator* or *one-shot*.

one clock tick (see figure 5.38). Thus, the output stays in high state during signal periods, but goes into low state immediately when the reference clock stops recharging the capacitor. It should be mentioned that the output has a very low leakage current of $I_{\mathrm{IL}} < 10\,\mu\mathrm{A}$ and has not to be considered for the discharging process. The output is then inverted inside the CPLD and fed into the PFD INHIBIT.

Figure 5.40 shows a picture of the CPLD and the soldered monoflop, and the resulting

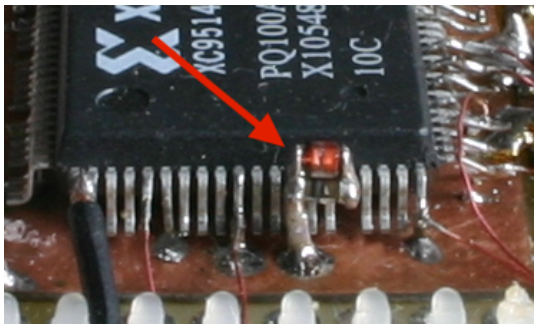


Figure 5.40: Close-up view of the monoflop. Diode and resistor are soldered directly on the pins, a capacitor is placed in vertical position from the input pin to the ground plate.

signals are presented in figure 5.41. When the reference clock (CH3, red) stops, the voltage of the monoflop drops exponentially and reaches $U_{\mathrm{IL}} = 0.8\,\mathrm{V}$ after $t \approx 40\,\mathrm{ns}$. Taking into account that the measuring probe of the oscilloscope has an additional capacitance of $\approx 8\,\mathrm{pF}$ to the implemented $C_{\mathrm{mono}} = 22\,\mathrm{pF}$, t_{real} should be slightly faster and close to the optimum of $t_{\mathrm{opt}} = 25\,\mathrm{ns}$ ($R = 1\,\mathrm{k}\Omega$).

5.4.5 Phase-Locked Loop and Filter Design

The filter design for a Phase-Locked Loop is far from trivial because of the unapparent balance of two properties of a filter: fast response and stability. Furthermore, this special case requires additional efforts due to the blanking time. The PLL has to run extremely stable during the blanking time, but also to react fast on phase differences when the reference clock sets in again. The aim is obviously to keep the unsynchronous periods as short as possible and to minimise jitter in general.

Three cases have to be managed: The ability to lock to a 40 MHz reference clock in general; the ability to achieve synchronisation after the relatively small blanking time at the HSYNC ($\sim 2.5\,\mu\mathrm{s}$); the ability to achieve synchronisation after the blanking time at VSYNC ($\sim 40\,\mu\mathrm{s}$). Figure 5.42 illustrates the blanking spaces after VSYNC and HSYNC. It should be mentioned that the fast synchronisation after the HSYNC is favourable because every clock tick t_{jitter} that is lost due to asynchronicity and jitter is multiplied by the number of lines on the screen

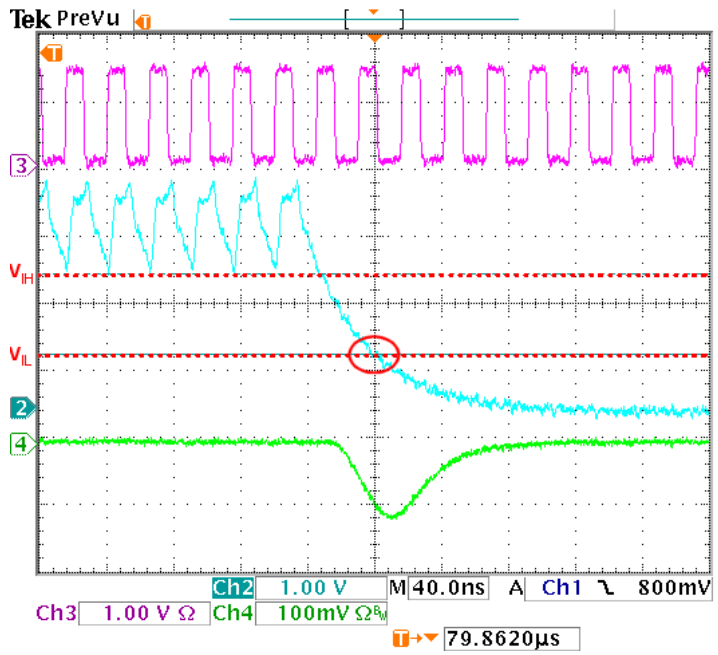


Figure 5.41: Scope view of the monoflop signal (CH2, cyan). When the blanking space begins, the clock stops and the capacitor of the monostable multivibrator discharges. Simultaneously the PFD starts to apply phase correction to the VCO input (CH4, green) until the voltage of the monoflop falls below $U_{\mathrm{IL}} = 0.8\,\mathrm{mV}$, which activates the PFD INHIBIT (indicated by the red circle). CH3 (pink) shows the basically unpertubated output of the VCO.

($n_{\mathrm{ticks}} \cdot 1200 \cdot 6.25\,\mathrm{ns} = n_{\mathrm{ticks}} \cdot 7.5\,\mu\mathrm{s}$), where on the other hand the consolidation phase after the VSYNC only affects the first one or two lines ($\sim 25\,\mu\mathrm{s}$).

Low-pass filters are a common passive implementation of a loop filter. Two types of low-pass filters have been considered, the lag filter, which is a basic low-pass filter consisting of a resistor in series and a capacitor to ground, and the lag-lead filter with an additional capacitor C_2 and a leak current compensation (see figure 5.43). Apart from general considerations on the design of the loop filter, the blanking space issue demands high values for the capacitor(s) in order to maintain the voltage at the VCO input during the blanking space. Another constraint for the filter is the maximum output current of PFD OUT with $I_{\mathrm{out,\,max}} = \pm 20\,\mathrm{mA}$ which results in

$$R_1 > \frac{U_{\mathrm{OH}}}{I_{\mathrm{out,\,max}}} = \frac{4.5\,\mathrm{V}}{20\,\mathrm{mA}} = 225\,\Omega.$$

The lag filter was tested and turned out not to be able to synchronise after the blanking

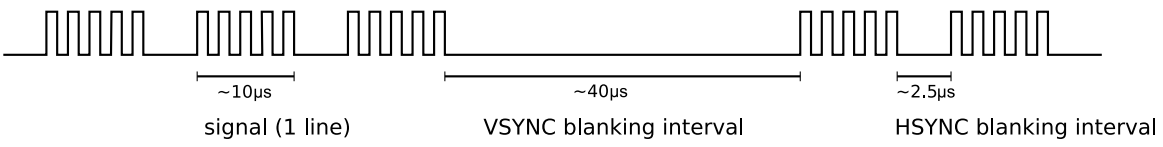


Figure 5.42: Illustration of the blanking spaces.

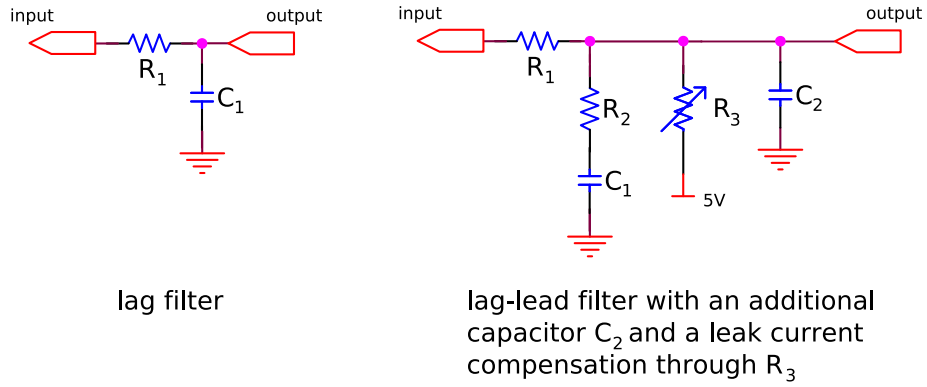


Figure 5.43: Low-pass filters considered for the PLL loop filter.

space with frequencies above 25 MHz. Therefore the lag-lead filter was introduced which has an additional resistor R_2 in series with the capacitor C_1 and another capacitor C_2 for noise compensation. R_2 damps the charging of C_1 which results in a faster response to changes of PFD OUT and better lock capabilities. Additionally, a loaded voltage divider was introduced in the loop in order to compensate leak currents at the VCO input, which cause a voltage drop and thus lead to decreased frequencies and larger corrections after the blanking space. The values for C_1, C_2, R_1 and R_2 can be calculated [38]. As the filter is in general very sensitive to parasitic capacities and hidden resistors, the final values have been evaluated by thorough variations of the quantities. Table 5.4 contains the result, i.e. the measured values. A block diagram of the final circuit is shown in figure 5.44.

Symbol	Value
C_1	470 pF
C_2	47 pF
R_1	$602 \pm 5\,\Omega$
R_2	$49.6 \pm 5\,\Omega$
R_3	$92 \pm 1\,\mathrm{k}\Omega$

Table 5.4: Lag-lead loop filter values

5.4.6 Board Performance and Summary

Figure 5.45 shows an oscilloscope picture of the situation after the blanking space of the horizontal synchronisation. The compensation of the leak currents is almost perfect, so that the reference clock (CH3, pink) and the VCO clock (CH2, cyan) are almost in phase and only a minor correction pulse over seven clock ticks and a small amplitude of $U_{\max} = 36\,\mathrm{mV}$ is necessary (CH4, green). The situation after the vertical synchronisation is different (figure 5.46). Here, the VCO input voltage is not sufficiently maintained (voltage drop of $\sim 20\,\mathrm{mV}$ during blanking space) and the phase difference requires a correction pulse with 100 mV and $t = 1\,\mu\mathrm{s}$. Also the second line after the VSYNC and another HSYNC blanking space is affected, though the correction pulse is already much smaller. Synchronicity is then guaranteed only from the

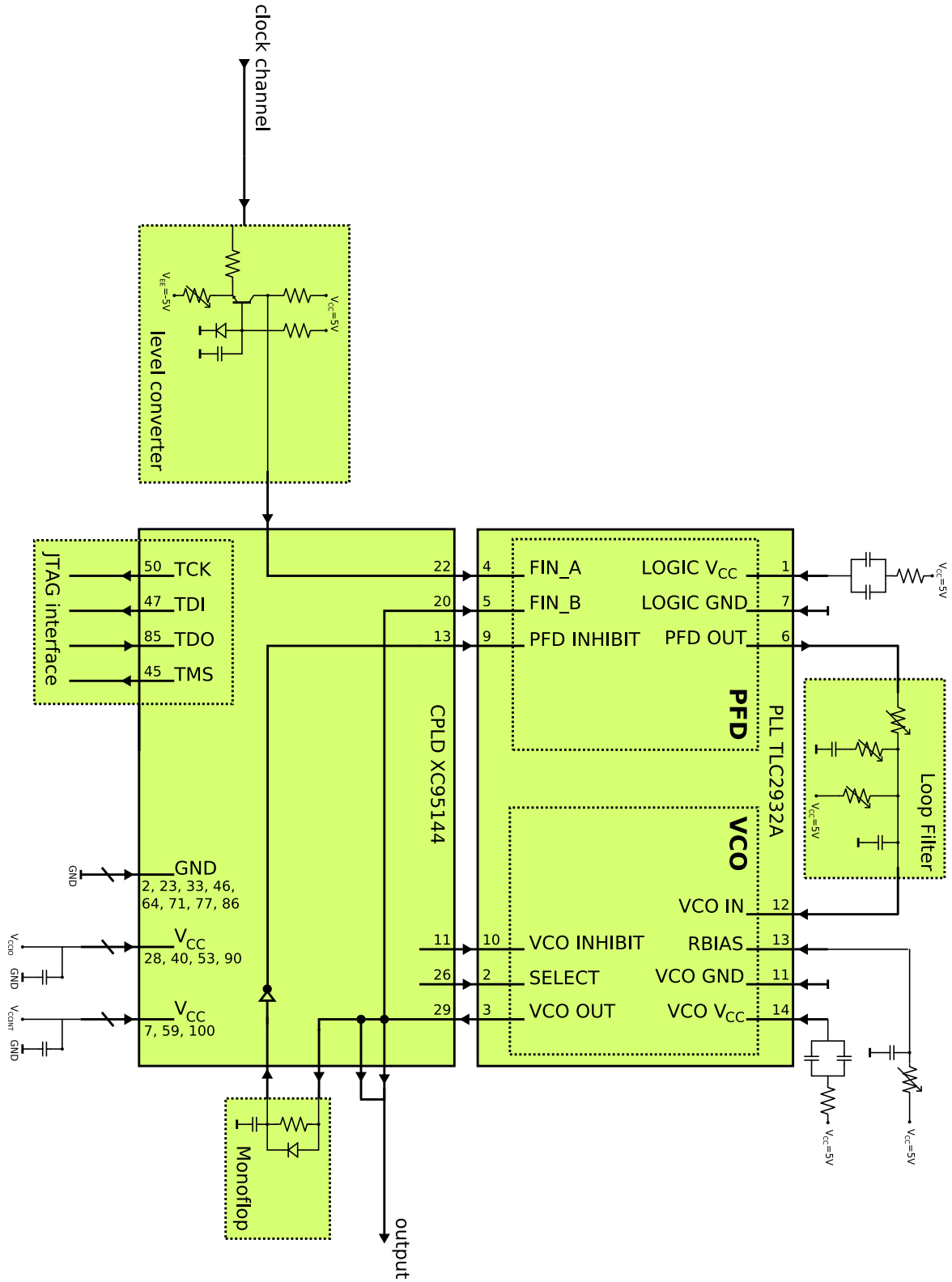


Figure 5.44: Block diagram of the clock synchronisation board.

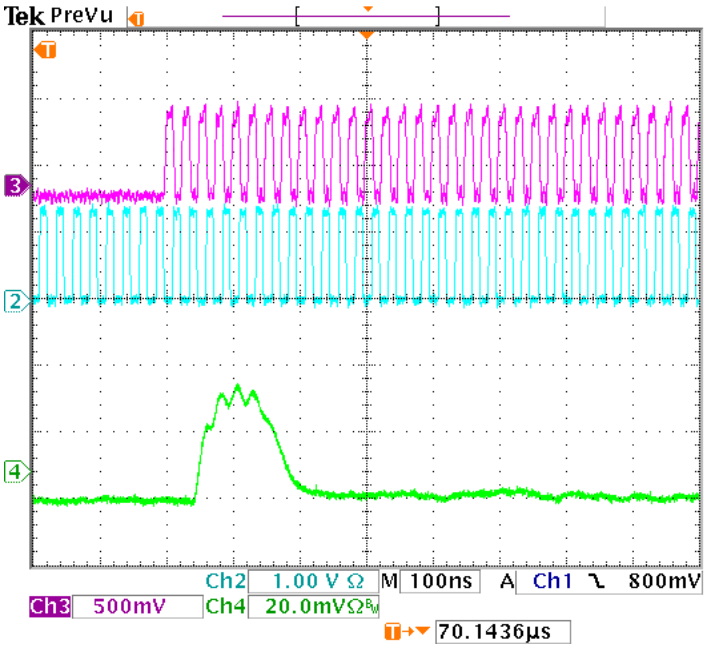


Figure 5.45: Synchronisation process after the blanking space of the horizontal synchronisation. Corrections (CH4, green) are very small ($U_{\max} = 36\,\mathrm{mV}$ over seven clock ticks), the signal from the VCO is almost in phase with the reference clock (CH3, pink).

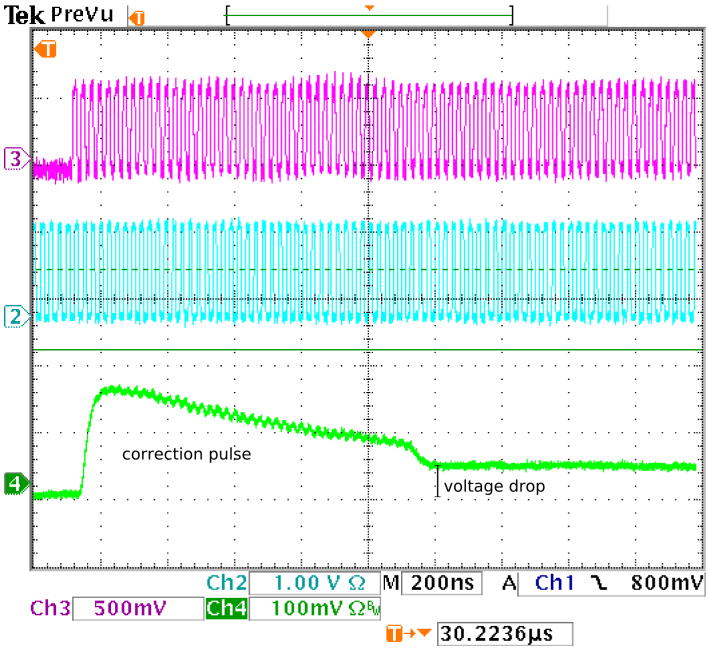


Figure 5.46: Synchronisation process after the blanking space of the vertical synchronisation. From the voltage drop it arises that the VCO input voltage is not maintained sufficiently. Therefore, the reference signal (CH3, pink) and the VCO signal (CH2, blue) are not in phase after the blanking space and a correction pulse (CH4, green) with a maximum amplitude of 100 mV and a length of 1 µs is applied.

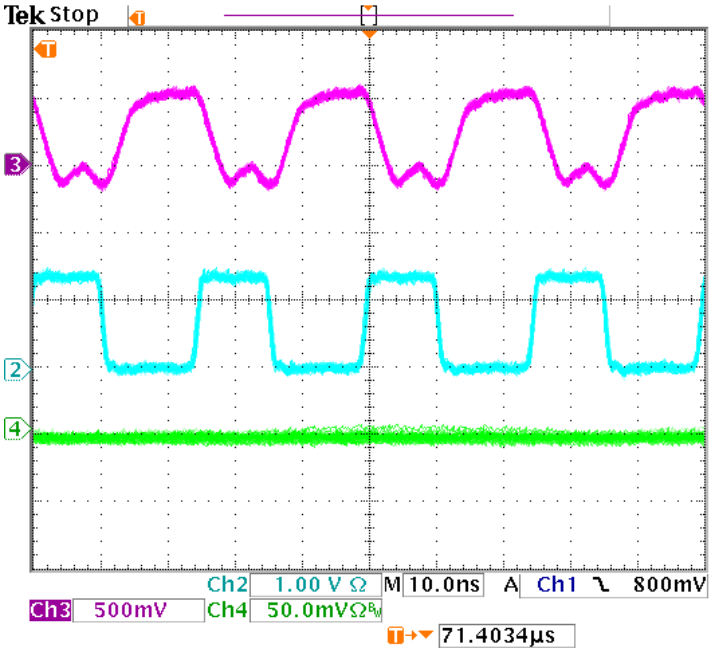


Figure 5.47: Scope view of the synchronised reference signal (CH3) and VCO output signal (CH2). The control voltage at VCO IN is constant.

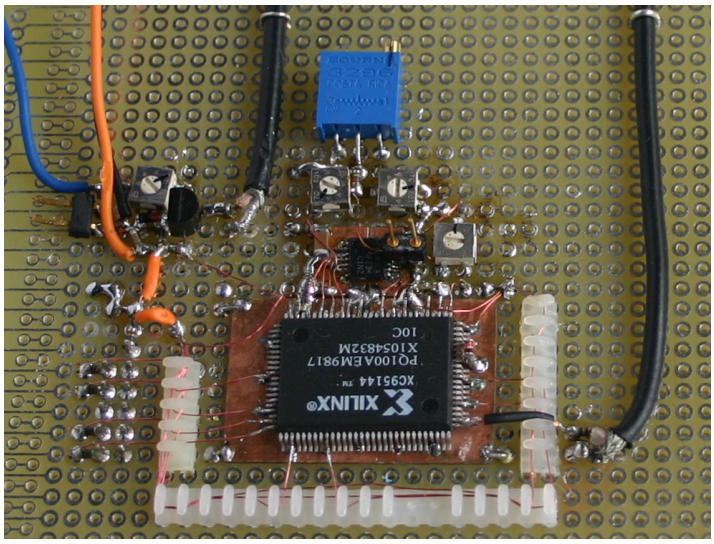


Figure 5.48: Picture of the final circuit of the Clock Synchronisation Board. It consists mostly of 0805 surface mount technology (SMT) components soldered on a blank board to keep the circuit compact. The CPLD and PLL packages where mounted on copper ground plates to guarantee stable working conditions. Ground pins are bent down such that they carry the chip with a small distance to the copper plate. Thus all supply voltages inputs can be blocked easily with capacitors between the pins and the ground plate.

third line, which corresponds to 25 µs after the VSYNC signal. As figure 5.47 shows, jitter after successful synchronisation is within 1 ns and is therefore negligible.

Figure 5.48 shows a picture of the *Clock Synchronisation Board*. The circuit was soldered on a blank board. In order to keep the circuit compact, mostly 0805[22] surface mount technology (SMT) components have been used. The npn-transistor of the level converter is a Motorola MPS 3563. The JTAG connector is mounted on the backside of the board and thus not visible. The CPLD and PLL packages where mounted on copper ground plates to guarantee stable working conditions, which is essential for a reliable synchronisation. Furthermore, all components are blocked thoroughly with 100 nF capacitors to reduce high frequency noise.

Concluding, the clock synchronisation is very stable apart from the first two lines after the vertical synchronisation, which has to be taken into account by software.

5.5 Measurement

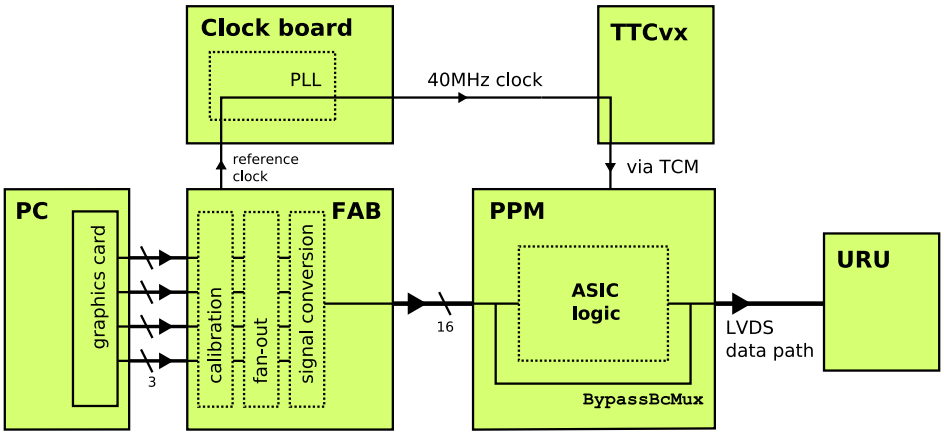


Figure 5.49: Block diagram of the test setup including the PPM, TTCvx and the *Universal Receiver Unit* (URU).

In order to verify the functionality of the test setup, it must be proven that the differential signals are received by the PPM and digitised correctly. This was achieved by setting up the complete signal chain including the PPM as decribed in the following.
The FAB was configured in 4-HEAD mode and operated with the same pulse sequence as in the preceding sections, including the offset to provide negative signals and the generation of the clock on channel 17. The clock signal is delivered to the clock board, which provides a stable 40 MHz reference clock synchronous to the graphics card signal. Both, the 16 differential output signals and the reference clock are provided to the PreProcessor Module test crate. The signals are connected directly to the PPM over the front panel input. The clock signal in contrast has to be distributed via the Timing and Trigger Control (TTC) system. Therefore, the clock signal is fed into the *TTCvx* module[23], which passes the clock via optical links to

[22] *0805* specifies the dimensions of the component in inches: $0.08'' \times 0.05''$ (2.0 mm × 1.25 mm).

[23] It should be noted that the conventional unit to supply the clock via an optical link is the *TTCex*. However, this is tuned to the exact bunch crossing frequency of 40.08 MHz and very restrictive on the frequency of the external clock (40.079 MHz ± 0.002 MHz) [39]. Therefore, the predecessor module *TTCvx* that also accepts a 40.00 MHz clock must be used.

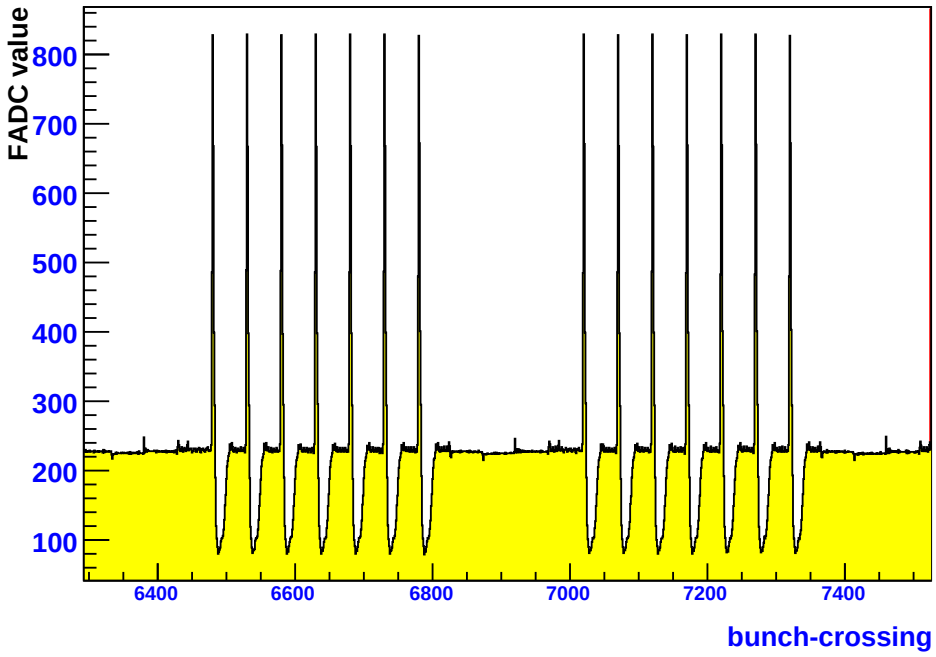


Figure 5.50: 10-bit digitised test pulses taken after the FADC using the BypassBcMux readout path. The shown time interval extends about 1000 BCs and 25 µs respectively.

parameter	FADC [# counts]	U_{FADC} [V]	U_{input} [V]
baseline	230	0	0
maximum	840	1.525	1.8
minimum	80	-0.375	-0.4
error	±10	±0.025	±0.1

Table 5.5: Corresponding voltages to the FADC counts and the respective values of the input signal (1 FADC count ≈ 2.5 mV).

the TCM. Based in the same crate as the PPM, the clock signal is finally transmitted to the PPM via the crate backplane.
Figure 5.49 shows the block diagram of the final setup. The PPrASIC provides the possibility to bypass the ASIC logic block for debugging purposes. When the register `BypassBcMux` is set, the incoming raw 10-bit digitised data from the FADC is passed directly to the LVDS serialiser output. The PPM LVDS output data is then analysed by the so-called *Universal Receiver Unit* (URU), which is a modular system of VME cards which stores the 10-bit data words on an internal memory with a depth of $2^{14} = 16\,384$ bunch crossings, i.e. $t_{\text{buffer}} = 409.6\,\mu\text{s}$.
Figure 5.50 shows the LVDS readout over a time interval of about 1000 BCs. It consists of two lines from graphics card's image pattern with seven identical pulses each and the blanking space in between. The baseline of the FADC window was chosen such that the undershoot is within the range. Table 5.5 lists the voltages corresponding to the FADC counts and the

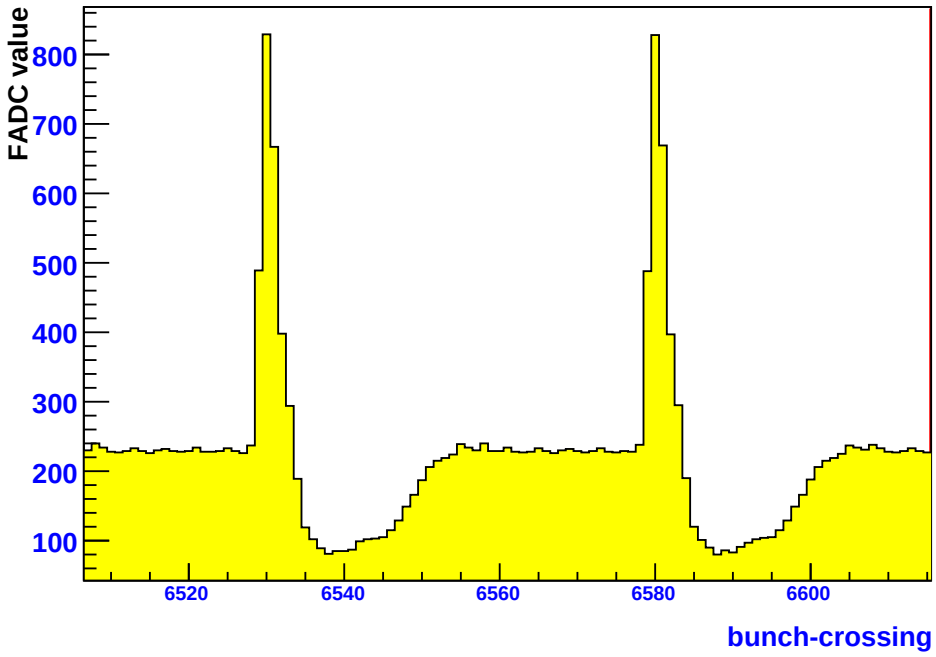


Figure 5.51: Test pulses in a range of about 100 bunch crossings. The similar digitization levels of two consecutive pulses demonstrate the synchronicity of the generated signals and the PPM sampling frequency.

voltages of the output stage from figure 5.28. The difference in the maximum amplitude of about 15% originates mainly from the sampling phase, since a calibration of the Phos4 chip was not performed (see section 3.2.2) and the pulse is probably not sampled at its maximum. Figure 5.51 shows two subsequent pulses in detail. The digitisation levels for both pulses are almost identical, which is a clear evidence that the sampling frequency of the PPM is synchronous with the generation of the signals, i.e. with the reference clock provided by the clock synchronisation board.

5.6 Summary

It was shown that the introduced test setup is a working alternative to commercially available signal generators as a fully controlled laboratory test environment to emulate the ATLAS Calorimeter signals for the PPM. As signal source, a commercial graphics card was chosen from a set of various, fully evaluated candidates. A dedicated software package that was developed in the course of this work allows the easy and straightforward modification and control of the signals. For the electrical conditioning, a generic printed circuit board was developed that includes a fan-out to 16 channels for various input configurations, and 64 channels in a future step. Furthermore, an additional device was built that generates a synchronous clock relatively to the signals, which has to be provided to the PPM as a reference. In a final measurement, the functionality ot the developed test setup was explicitly confirmed.

Chapter 6

Summary and Outlook

The Rate Metering and Histogramming functionality of the PreProcessor System of the ATLAS Level-1 Calorimeter Trigger is a valuable instrument which allows to monitor the input rates from the calorimeter with high statistics unbiased from trigger decisions. This thesis is concerned with the determination of the input rates as expected in the final experiment, based on the full simulation of the occurring physics and the detector properties. Moreover, a generic test setup was developed to study the properties of the Rate Metering system, including the development of a software package, electronic circuit design, the implementation as printed circuit board, soldered circuitry and the thorough evaluation of the used components.

The analysis is concerned with the systematic study of the rates as they are expected during operation of the experiment. The dependency on luminosity, different time intervals for the readout frequency and the threshold energy was shown. On that basis, sets of parameters were acquired exemplarily for various purposes in the early and later stages of the experiment. These usage scenarios give a good impression of the Rate Metering and Histogramming functionality in the final experiment.

A test setup was developed to test the functionality of the hardware implementation of the Rate Metering and Histogramming. It comprises the generation of analogue signals in order to emulate the signal pulses from the ATLAS calorimeters. The first stage is a graphics card that generates signals with the basic shape of pulses from the TITAN pulse library. A software package, consisting of two parts, was developed to control the graphics card's output. The `Signal Builder` software offers a graphical user interface to adequately modify the pulses with respect to amplitude, virtual baseline and timing and to arrange them in sequences. Merged into rgb-images, these sequences are generated at the graphics card's output using the `displayFS` programme.

The properties of commercial graphics cards were studied in terms of linearity, noise, crosstalk and synchronisation of the output channels. It was shown that they are well suited for the desired purpose. Part of the investigation also was the inter-synchronisation of multiple graphics cards. However, the required precision turned out not to be achievable with the current possibilities of commercially available systems.

With the Fan-out and Amplification Board, a printed circuit board was developed to transform the unipolar, single-ended signals of the graphics card to differential signals with the correct voltage levels for the PreProcessor Module input. The board concept allows to use different input configurations depending on the available number of graphics card outputs and

provides 16 channels in either mode, and up to 64 channels in the yet untested stack mode. Moreover, the development of the FAB gave important know-how for future enhancements of the test system and new approaches in the generation of analogue signals as part of the PreProcessor commissioning and maintenance.

In order to guarantee synchronicity between the simulated signals and PPM hardware, whose clock rate is related to the LHC bunch crossing frequency, the test setup includes the generation of a 40 MHz reference clock. The problem of the blanking space, being an intrinsic property of the graphics card, was encountered with the clock synchronisation board that uses a PLL in combination with a CPLD and a monoflop to provide a clock which is stable over time with a jitter below 1 ns.

The functionality of the test setup was proven in a measurement by reading out the generated pulses as digitised FADC counts from the PreProcessor Module, which reflected the correct pulse shape and the synchronicity of signal and clock. Although it was not possible to provide 64 independent signals, the test setup with commercial graphics cards acting as signal generator turned out to be a working concept to emulate the pulses of the ATLAS calorimeters.

Future studies will include the analysis of rates with respect to the calibration of the ATLAS calorimetry utilising the very high statistics that can be achieved with the Rate Metering. Similarly, effects from beam parameters should be investigated to evaluate the feasibility of drawing conclusions e.g. from asymmetric rate distribution on the beam alignment.

After the verification of the examination of the yet untested stack mode of the Fan-out and Amplification board and an adjustment of the frequency characteristics, the integration into the module tests of the PreProcessor System is the next big step. The resulting comprehensive test setup will allow to verify all analogue components of the PreProcessor Module including the evaluation of the functionality of the Rate Metering hardware implementation in a fully controlled laboratory environment.

Appendix A

Software

A.1 PC System Configuration

component	driver	version
linux kernel		linux-2.6.22-gentoo-r10
X-Server	Xorg	1.1.1-r5
	X11	7.1
Matrox QID Pro	mtx_drv	x86_64-1.4.5

Table A.1: Overview of the used drivers and versions of the graphics card host system.

The X-Server should be started with the following parameters:
`X :1 -config /etc/X11/xorg.conf.QID -sharevts -isolateDevice PCI:i:j:k -keeptty -ac -noreset -dpms -verbose`,
where `xorg.conf.QID` is the configuration file of the X-Server, based on the driver documentation (see table A.1), and `PCI:i:j:k` is the hardware ID of the graphics card.

A.2 displayFS

NAME

`displayFS` - display images on a (black) fullscreen

SYNOPSIS

```
displayFS [options] image1 screen1 x1 y1 image2 screen2 x2 y2 ...
```

DESCRIPTION

`displayFS` displays images on an X11-Server. It paints directly on the desktop unaware of any underlying menu bars etc. using TrollTech's qt4 GUI. Any drawing starts with painting the target screen background black.
Up to 24 images can be added to the command line in the format `[image screen x y]`.

`image`	image to be displayed
`screen`	specifies the screen of the target system
`x, y`	(x, y) specifies the position (top-left coordinate) of the image at the target screen.

POSIX OPTIONS

`-display :display`
: inherited from qt4; sets the X display (default is $DISPLAY). Use this option to specify the target X-Server **(RECOMMENDED)**

`-probeonly`
: causes the program to exit after loading images, check their properties, probing the target X-Server and print out this information

EXAMPLE OF USE

```
genfs -display :1 image1.png 1 0 0 image2.png 1 1600 0
```

will display `image1.png` on the X-Server running as DISPLAY :1 on screen #1, starting at coordinate (0, 0) and `image2.png` starting at coordinate (1600, 0). The example assumes a configuration of the X-Server at display :1 with 2 screens, each with a geometry of 3200x1200px.

NOTE

Remote use with `-display :display` recommended. Do not use on the X-Server you work with as target. The black background occupies the whole screen and takes most controlling possibilities from the user.

Program formerly named genfs.

AUTHOR

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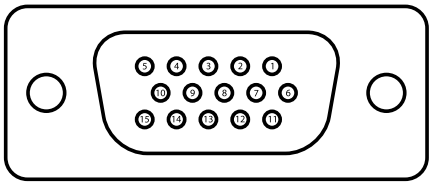
Appendix B

Hardware

B.1 Fan-Out and Amplification Board (FAB)



PIN	COMMENT
1	RED
2	GREEN
3	BLUE
5	GND HSYNC
6	GND RED
7	GND GREEN
8	GND BLUE
10	GND VSYNC
13	HSYNC
14	VSYNC

Figure B.1: Pinning of the VGA input connector [40].

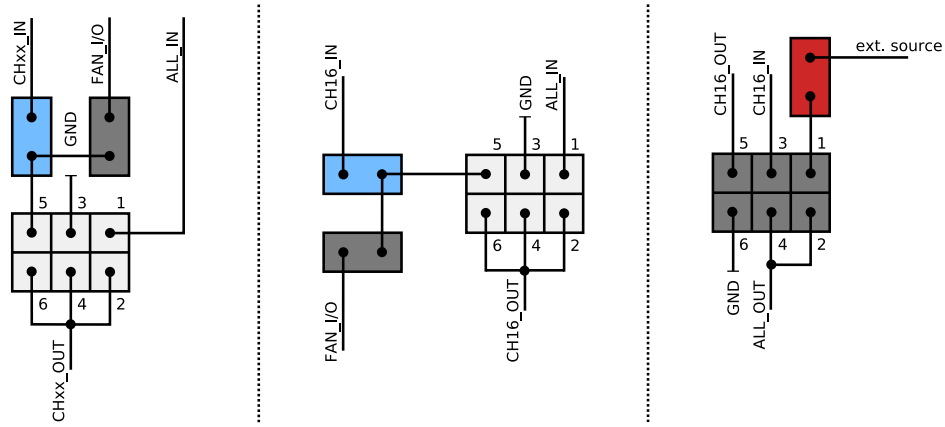


Figure B.2: Jumper setting of the FAB. On the left side, the jumper settings of a standard channel is shown. The middle column shows the setting at CH16, and the right side is the jumper setting for the input selection at CH16 respectively the external input.

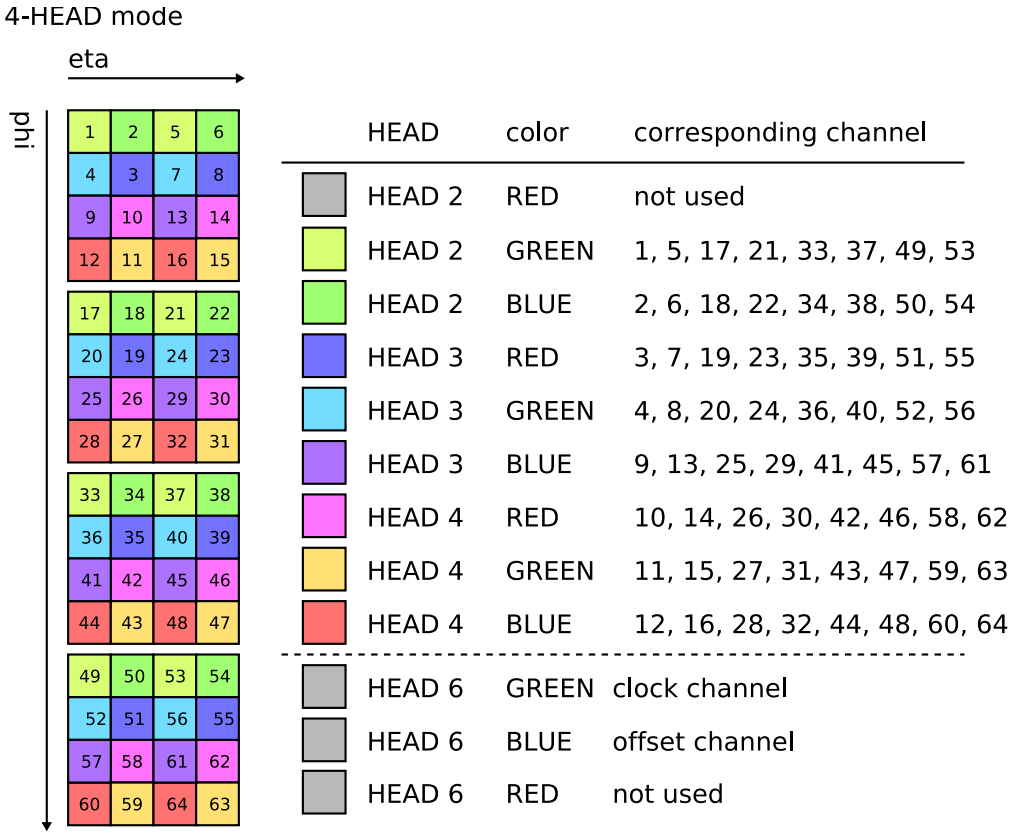


Figure B.3: Fan-out scheme of the FAB in 4 HEAD mode. 8 indipendent channels are arranged to a subset of a 2×4 bin area in $\eta \times \phi$ and reproduced several times, as indicated by the colours.

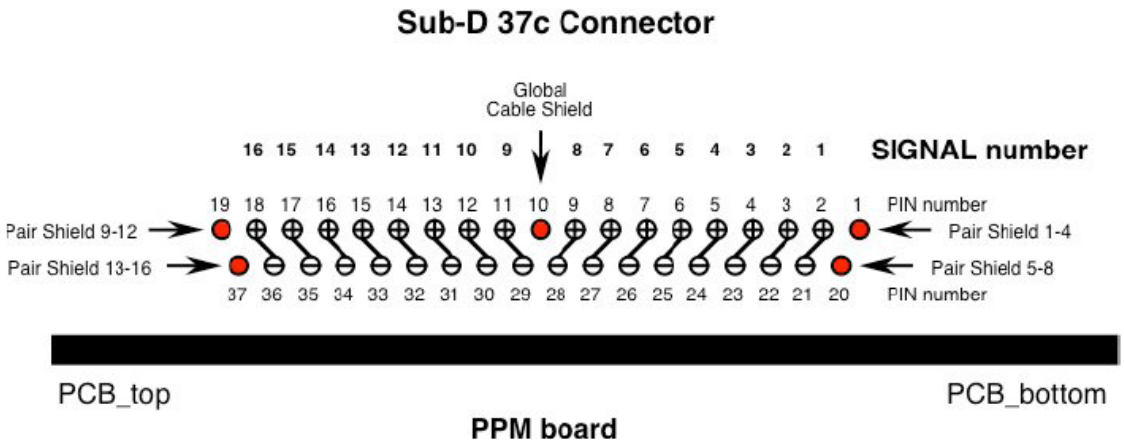


Figure B.4: FAB output connector. The differential pairs are indicated by lines between the + and − pins. Red marked pins are connected to ground-shields.

B.2 Pinning of the Clock Synchronisation Board Components

Name	I/O	#PIN	Description
PFD			
LOGIC V_{DD}	I	1	
FIN_A	I	4	reference clock f_{ref}
FIN_B	I	5	f_{VCO} from VCO
PFD OUT	O	6	Phase frequency detector result
LOGIC GND	I	7	
TEST	?	8	Connected to GND
PFD INHIBIT	I	9	Sets PDF OUT to high-impedance state if high
VCO			
SELECT	I	2	VCO output frequency select; 1/2 frequency if high
VCO OUT	O	3	f_{VCO}
VCO INHIBIT	I	10	Sets VCO OUT to low state if high
VCO GND	I	11	
VCO IN	I	12	Input from loop filter
RBIAS	I	13	An external resistor R_{bias} between VCO V_{DD} and RBIAS to adjust the VCO oscillation frequency; Blocked to GND
VCO V_{DD}	I	14	

Table B.1: PLL I/O connections (Texas Instruments, TLC2932A [36]).

Name	I/O	#PIN	Description
VCO_INH	O	11	Sets VCO_OUT to low state if high
PFD_INH	O	13	Sets PDF_OUT to high-impedance state if high
FIN_B	O	20	looped through clock f_{VCO} from VCO
FIN_A	O	22	looped through reference clock f_{ref}
VCO_OUT	I	24	f_{VCO} from VCO
SELECT	O	26	VCO output frequency select; 1/2 frequency if high
CLK_CH	I	29	f_{ref} from level converter / graphics card
JTAG communication			
TCK	I	50	
TDI	I	47	
TDO	O	85	
TMS	I	45	
GND	I	2, 23, 33, 46, 64, 71, 77, 86	
V_CCIO 3.3V/5V	I	28, 40, 53, 90	
V_CCINT 5V	I	7, 59, 100	

Table B.2: CPLD I/O connections (Xilinx, XC95144 [37]).

B.3 Generation of L1A

The generation of a L1A signal is not implemented in the original design of the FAB / clock board combination. To test the PPM in an offline setup, i.e. without JEM, CP, CTP and therefore without the normal L1A decision chain, an artificial L1A has to be provided by the test setup in order to trigger the readout. This signal must be transmitted after a fixed time interval related to the signal.
This can be achieved by several approaches, but small hardware modifications are needed:

Dedicated Channel

The most evident method would be to dedicate another channel to the generation of the L1A. This is possible for example in 4-HEAD mode with the unused CH16, but would need a patch cable from the input of CH16 to the clock board. The signal then should be processed in the same way as the clock signal (level converter, CPLD).
Advantage: free configurable in the order of the time resolution of the graphics card.
Disadvantage: patch and solderworks required, costs a channel, $f_{\text{min}} = f_{\text{VSYNC}}$ if no divide-by-N is used.

Deduction from clock signal, HSYNC and VSYNC

Another approach would be based on the synchronisation channels of the graphics card and use the CPLD as a counter. Therefore, HSYNC and VSYNC had to be provided to CPLD. The CPLD then could be programmed such that it derives a L1A output by counting a predefined number of ticks with HSYNC and VSYNC as starting reference. This has obviously to be in time with the signals.
Advantage: simple modifications, f_{min} can be configured.
Disadvantage: not very flexible, always a fixed pulse is triggered (if the CPLD is not programmed such that it alternates timing and thus trigger pulses in a rotative way).

Deduction from Clock Signal

Assuming that the PLL runs stable even when some clock ticks are missing, the L1A could be encoded within the clock signal. Therefore, the duration of the PFD INHIBIT period would have to be measured and, if below a certain limit (1 clock tick), a L1A would be triggered.
Advantage: very elegant because of minimal modifications.
Disadvantage: could cause instability, problematic since no reference clock is available during blanking space (compare section 5.4.4).

External Tool

An external tool could be applied to measure pulse heights of the generated signals and produce a L1A if above a given threshold.
Advantages: Stable if threshold is chosen wisely.
Disadvantages: Threshold is fixed, only high pulses can be triggered.

List of Figures

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Bibliography

[1] Donald H. Perkins. *Introduction to High Energy Physics*. Addison Wesley, third edition, 1987.

[2] Stephen P. Martin. *A Supersymmetry Primer*, 2006. hep-ph/9709356v4.

[3] Lisa Randall, Raman Sundrum. *A Large Mass Hierarchy from a Small Extra Dimension*, 1999. hep-ph/9905221v1.

[4] Peter W. Higgs. *Broken symmetries, massless particles and gauge fields*, 1964. Phys. Lett. 12, 132.

[5] L3 OPAL the LEP Electroweak Working Group The LEP Collaborations: ALEPH, DELPHI. *A Combination of Preliminary Electroweak Measurements and Constraints on the Standard Model*, 2007. hep-ex/0612034v2.

[6] ATLAS Collaboration. *ATLAS Detector and Physics Performance*, 1999. Technical Design Report CERN/LHCC/99-14, CERN.

[7] AC Team. *Overall view of the LHC experiments*, 1999. CERN-AC-9906026, `http://www.atlas.ch`.

[8] ATLAS Inner Detector Collaboration. *Inner Detector*, 1997. Technical Design Report CERN/LHCC/97-16, CERN.

[9] Ullrich Pfeiffer. *A Compact Pre-Processor System for the ATLAS Level-1 Calorimeter Trigger*. PhD thesis, Institut für Hochenergiephysik, Universität Heidelberg, 1999.

[10] ATLAS Calorimeter Performance Collaboration. *Calorimeter Performance*, 1997. Technical Design Report CERN/LHCC/96-40, CERN.

[11] ATLAS Tile Calorimeter Collaboration. *Tile Calorimeter*, 1996. Technical Design Report CERN/LHCC 96-42, CERN.

[12] ATLAS Muon Collaboration. *Muon Spectrometer*, 1997. Technical Design Report CERN/LHCC 97-22, CERN.

[13] ATLAS Collaboration. *The ATLAS Experiment at the CERN Large Hadron Collider*, 2008.

[14] R. Achenbach et al. *The ATLAS Level-1 Calorimeter Trigger*, 2008. JINST 3 P03001.

[15] ATLAS Liquid Argon Calorimeter Collaboration. *Liquid Argon Calorimeter*, 1996. Technical Design Report CERN/LHCC/96-42, CERN.

[16] Paul Hanke. *The Pre-Processor Module (PPM) for the ATLAS Level-1 Calorimeter Trigger*, 2008.

[17] Pavel Weber. *ATLAS Calorimetry: Trigger, Simulation and Jet Calibration*. PhD thesis, Kirchhoff Institute for Physics, University of Heidelberg, 2008.

[18] B. Hallgren. *Controller Area Network - hardware description*. `http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/DCS/CANINFO/canhard.htm`.

[19] Victor Andrei. *PPM Firmware, recent developments*, 2008. L1Calo Trigger Joint Meeting, Birmingham.

[20] Torbjörn Sjöstrand et al. *PYTHIA*. `http://home.thep.lu.se/~torbjorn/Pythia.html`.

[21] Allison, J. et al. Geant4 developments and applications. *IEEE Transactions on Nuclear Science*, 2006.

[22] ATLAS Computing Group. *ATLAS Detector and Physics Performance*, 2005. Technical Design Report CERN-LHCC-2005-022, CERN.

[23] Victor Lendermann. *Dijets: uniformity in jet response*, 2008. 4^{th} ATLAS Hadronic Calibration Workshop.

[24] Alan Watson. *Private email correspondence*.

[25] nVidia Corporation. *Genlock*. `http://www.nvidia.com/object/IO_10793.html`.

[26] nVidia Corporation. *NVIDIA Quadro G-Sync*, 2006. `http://www.nvidia.com/page/quadrofx_gsync.html`.

[27] Matrox Inc. *Matrox Advanced Synchronisation Module*, November 2003.

[28] Hasko Stenzel. *Trigger Tower Analogue Signal Library*, November 2001.

[29] Inc. Trolltech. *Qt, the cross-platform C++ GUI toolkit*. `http://trolltech.com`.

[30] Paul Horowitz and Winfield Hill. *The Art Of Electronics*. Cambridge University Press, second edition, 1989.

[31] Texas Instruments Incorporated. *OPA820 Unity-Gain Stable, Low-Noise, Voltage-Feedback Operational Amplifier*, March 2006.

[32] Linear Technology Corporation. *LT1813 Dual/Quad 3mA, 100MHz, 750V/us Operational Amplifiers*, 2001.

[33] Texas Instruments Incorporated. *OPA650 Wideband, Low Power Voltage Feedback Operational Amplifier*, 2005.

[34] *Cadence Design Systems, Inc.* `http://www.cadence.com`.

[35] *Würth Electronik GmbH & Co. KG*. `http://www.wuerth-elektronik.de`.

[36] Texas Instruments Incorporated. *TLC2932A High-Performance Phase-Locked Loop*, October 2005.

[37] Inc. Xilinx. *XC95144 In-System Programmable CPLD*, April 2006.

[38] Texas Instruments Incorporated. *TLC2932A High-Performance Phase-Locked Loop*, May 1997.

[39] B.G. Taylor. *TTC laser transmitter (TTCex, TTCtx, TTCmx) User Manual*.

[40] *DE15 Connector Pinout*. `http://de.wikipedia.org/wiki/Bild:DE15_Connector_Pinout.svg`.

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Erklärung:

Ich versichere, daß ich diese Arbeit selbständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den 30.04.2008

.....
(Unterschrift)